

N5991MM5A MIPI M-PHY® 5

Receiver Compliance Test Automation Software

The screenshot displays the MIPI M-PHY N5991 ValiFrame software interface. The main window is divided into a left sidebar for test configuration and a right pane for test details and results.

Left Sidebar (Test Configuration):

- MIPI M-PHY - 5.00**
 - Calibration
 - HS Tests
 - HS Terminated Tests
 - Terminated Mode 23.296 GBit/s
 - Test 2.1.1 - HS-RX Differential Input Voltage Amplitude (V_{DIF-DC-HS-RX}) Data0 at 23.296 GBit/s
 - Test 2.1.3 - HS-RX Common-Mode Input Voltage Tolerance (V_{CM-RX}) Data0 at 23.296 GBit/s
 - Test 2.1.8 - HS-RX Prepare Length Capability Verification (T_{HS-PREPARE-RX}) Data0 at 23.296 GBit/s
 - Test 2.1.9 - HS-RX Sync Length Capability Verification (T_{SYNC-RX}) Data0 at 23.296 GBit/s
 - Test 2.1.2 - HS-RX Accumulated Differential Input Voltage Tolerance (V_{DIF-ACC-HS-GX-RX}) Data0 at 23.296 GBit/s
 - Test 2.1.7 - Receiver Jitter Tolerance (T_{JRX}, D_{JRX}, R_{JRX}, S_TT_{JRX}, S_TD_{JRX}) Positive Offset Data0 at 23.296 GBit/s**
 - Test 2.1.7 - Receiver Jitter Tolerance (T_{JRX}, D_{JRX}, R_{JRX}, S_TT_{JRX}, S_TD_{JRX}) Negative Offset Data0 at 23.296 GBit/s
 - Test 2.1.4 - HS-RX Differential Termination Enable Time (T_{TERM-ON-HS-RX}) Data0 at 23.296 GBit/s
 - Test 2.1.5 - HS-RX Differential Termination Disable Time (T_{TERM-OFF-HS-RX}) Data0 at 23.296 GBit/s
 - Squelch Tests
 - Test 2.4.3 - SQ-RX Squelch Exit Voltage (V_{SQ}) Data0
 - Test 2.4.4 - SQ-RX Squelch Exit Time (T_{SQ}) Data0
 - Test 2.4.5 - SQ-RX Squelch Noise Pulse Width (T_{PULSE-SQ}) Data0
 - Test 2.4.6 - SQ-RX Squelch Noise Pulse Spacing (T_{SPACE-SQ}) Data0
 - PWM Tests
 - PWM Non-Terminated Tests
 - PWM Non-Terminated Mode Gear1
 - Test 2.2.1 - PWM-RX Differential DC Input Voltage Amplitude (V_{DIF-DC-PWM-RX}) Data0 at Gear1
 - Test 2.2.2 - PWM-RX Common-Mode Input Voltage Tolerance (V_{CM-RX}) Data0 at Gear1
 - Test 2.2.5a - PWM-RX Receive Bit Duration Tolerance (TOLPWM-RX) Data0 at Gear1
 - Test 2.2.5b - PWM-RX Receive Bit Duration Tolerance, During LINE-READ (TOLPWM-G1-RX) Data0 at Gear1
 - Test 2.2.6 - PWM-RX Receive Ratio for PWM-G1 (kPWM-RX) Data0 at Gear1
 - PWM Terminated Tests
 - PWM Terminated Mode Gear1
 - Test 2.2.1 - PWM-RX Differential DC Input Voltage Amplitude (V_{DIF-DC-PWM-RX}) Data0 at Gear1
 - Test 2.2.2 - PWM-RX Common-Mode Input Voltage Tolerance (V_{CM-RX}) Data0 at Gear1
 - Test 2.2.3 - PWM-RX Differential Termination Enable Time (T_{TERM-ON-PWM-RX}) Data0 at Gear1
 - Test 2.2.4 - PWM-RX Differential Termination Disable Time (T_{TERM-OFF-PWM-RX}) Data0 at Gear1
 - Test 2.2.5a - PWM-RX Receive Bit Duration Tolerance (TOLPWM-RX) Data0 at Gear1
 - Test 2.2.5b - PWM-RX Receive Bit Duration Tolerance, During LINE-READ (TOLPWM-G1-RX) Data0 at Gear1
 - Test 2.2.6 - PWM-RX Receive Ratio for PWM-G1 (kPWM-RX) Data0 at Gear1
 - Interference Tests
 - Interference Calibration
 - Test 2.4.7 - SQ-RX Squelch RF Interference Tolerance (V_{INT-SQ}, f_{INT-SQ}) Data0
 - Common Mode Interference at 23.296 GBit/s

Right Pane (Test Details):

Test 2.1.7 - Receiver Jitter Tolerance (T_{JRX}, D_{JRX}, R_{JRX}, S_TT_{JRX}, S_TD_{JRX})

- Offline: True
- Compliant: False
- Attenuator: 0 dB
- Lane Under Test Termination: T1000hm
- Stall length: 20
- Initial Adapt Length: 0
- Initial Adapt Type: Fine
- Refresh Adapt Length: 0
- Refresh Adapt Type: Fine
- LS Prepare length: 7
- Sleep length: 5
- PtM Tail of Burst: 10
- Reset Pulse Width: 100 us
- PtM Burst Closure Extensio: 32
- Ref Clock Frequency: 26 MHz
- Target BER: 1E-12
- IBERReader Init Mode: Data0, 23.296 GBit/s; RT
- Voltage Levels: Calibrated
- Retrial Number: 2
- Test Sequence: MPhyCompliance.seq
- Re-Init sequence after Reset: True
- Show Dialog at UniPro Rese: False
- HS Prepare Length: 15
- HS Sync Length: 7
- SJ Frequencies [MHz]: 1.6;16;20;26;26;500
- Common-Mode Voltage Leve: 0.18;0.025;0.33
- Frequency Offset: 150 ppm
- Accumulated Voltage Eye O: 37.5 mV
- Perform Jitter Limit Test: False

Equalization Settings

- AC Gain at Gear5: 11.856 dB
- DC Gain at Gear5: 1.75 dB
- Zero Frequency at Gear5: 2.06 GHz
- Pole 1 Frequency at Gear5: 6.59 GHz
- Pole 2 Frequency at Gear5: 20 GHz
- DFE Voltage Level at Gear5: 0 V

Error Detector

- Coupling: DC
- Termination Configuration: Unbalanced
- Input range: 600 mV
- Common mode voltage: 200 mV

Sequencer

- Procedure Error Case Behav: Abort Sequence
- Procedure Failed Case Behv: Proceed With Next Procedure
- Repetitions: 0

Repetitions

Log:

Severity	Message	Date
Progress	Instrument Connections	11/9/2022 5:15:27 PM
Progress	Not opening connection to DSO Infinium Series because it is configured to be offline.	11/9/2022 5:15:27 PM
Progress	Not opening connection to Keysight M8040A J-BERT because it is configured to be offline.	11/9/2022 5:15:27 PM
Progress	Not opening connection to BIT-3000A because it is configured to be offline.	11/9/2022 5:15:27 PM
Info	MIPI M-PHY N5991 ValiFrame startup complete!	11/9/2022 5:15:29 PM

Status Bar: Ready | Warnings: 1 | SW Maintenance License is OK | Not Running

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At a Glance

High-speed digital standards are quickly evolving to keep pace with emerging technologies such as 5G, Internet of Things (IoT), artificial intelligence (AI), virtual reality (VR), and autonomous vehicles.

Each generational change introduces new test challenges for your digital designs. You need to test your high-speed digital designs across all product development stages — from design and simulation to analysis, debugging, and compliance testing. The N5991 product line anticipates test challenges, optimizes performance, and accelerates time-to-market of your high-speed computing interfaces, data-center connections, and consumer electronics.

- Supported standards include PCIe, SAS, SATA, USB, HDMI, DisplayPort, MIPI M-PHY® and MIPI C-PHY®. Other standards will be continuously added with the requirements for higher data-speed testing
- Guided setup with automated fast stress signal calibration and compliance measurement functions
- Modern look and feel with enhanced functionalities
- System modularity allows the user to enable only required functionalities
- HTML reports
- Node-locked and transportable licenses
- Characterization mode for in-depth testing
- Single- and multi-lane device testing

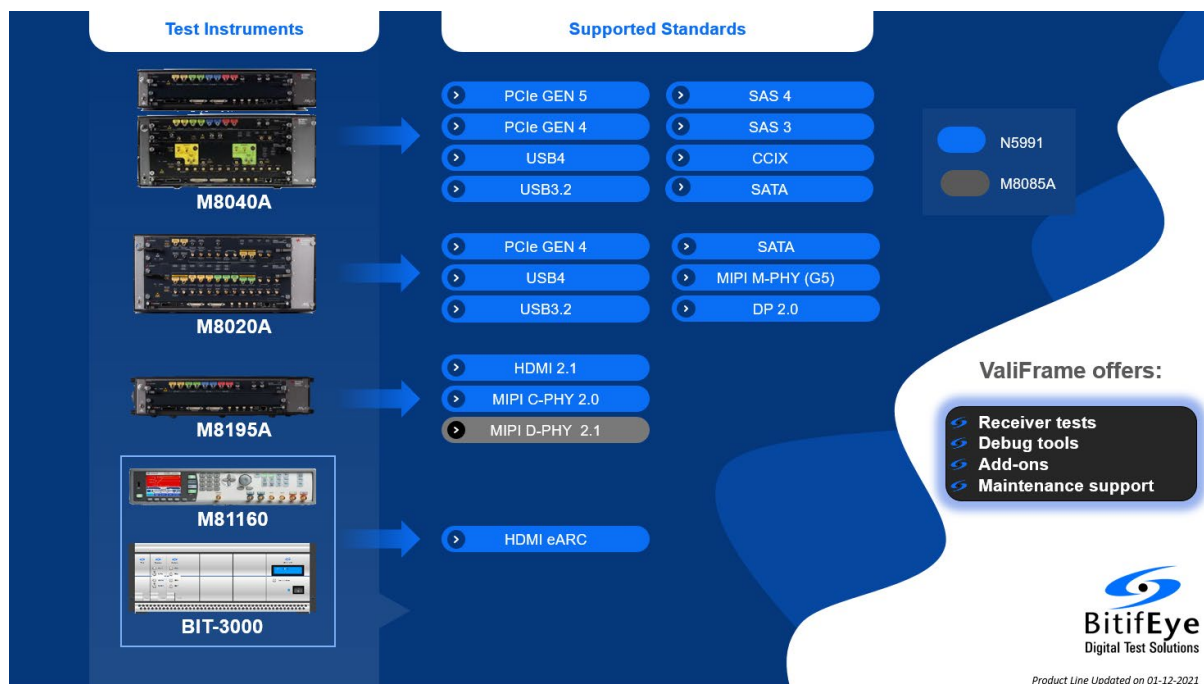


Figure 1. N5991 Software Solution Path

NOTE: This datasheet outlines the covered tests, instrument requirements and requirements for the PC the test automation software is running on.

Turn Your Instruments into a Solution

An efficient test strategy is a proven competitive advantage. The Keysight Technologies N5991 is the successor to the well-known industry standard N5990A test automation software platform. It follows the same concept – combining the performance of your instruments with the convenience of your PC. The system's software provides unprecedented test integration, high-throughput, and ease-of-use for a wide range of stimulus and response systems, providing a level of control that transforms a collection of instruments into a universal, user-friendly and highly productive test solution.

Standardize Your Tests

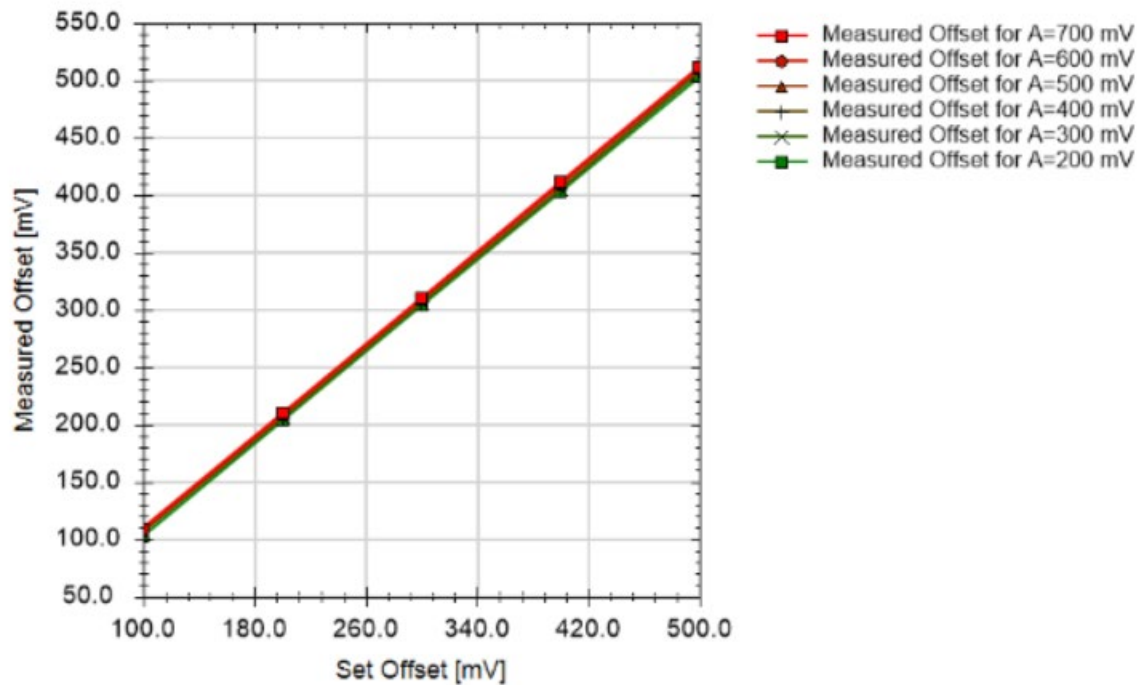
The N5991 receiver-test options provide dedicated receiver compliance tests for popular and emerging digital buses. The user can choose compliance mode for fast reassurance, or characterization mode for in-depth analysis. The Receiver Test Automation Platform's compliance testing capabilities have been repeatedly proven at interoperability workshops ("plug fests"). The N5991 builds on the success of previous generations to deliver significant gains in productivity. Like its predecessor, the N5990A, the new system makes it easy to test multiple buses by using the same interface for all available standards. It delivers additional gains by using familiar HTML for reporting results.

Test Selection and Test Results

The test automation software platform lets you select tests from an intuitive tree structure with multiple levels of detail. Select the tests you want to run, together with the number of repetitions. Test results are provided in HTML format. When you measure a parameter range, it delivers a specific graph and a related data table (see Figure 2).

Reference Clock Calibration Offset

Calibration of the generator Offset Terminated



```

----General-----
Offline                               False
Compliant                             False
Capture screenshot for each calibration measurement False
Amplitude Range                       0.2; 0.7; 5; Linear
Offset Range                           0.1; 0.5; 5; Linear
Run without TTC                        False
Wait for Manual Break                  False
Show DUT Configure Dialog              False
Sampling Rate                          Default
TrigThreshold Mode                     Auto
  
```

Set Offset [mV]	Measured Offset for A=700 mV [mV]	Measured Offset for A=600 mV [mV]	Measured Offset for A=500 mV [mV]	Measured Offset for A=400 mV [mV]	Measured Offset for A=300 mV [mV]	Measured Offset for A=200 mV [mV]
100	109	110	108	107	106	103
200	210	210	209	206	206	205
300	310	310	309	307	306	305
400	411	410	409	405	405	404
500	511	511	511	508	506	504

Figure 2. Test results for Reference Clock Calibration Offset

N5991MM5A M-PHY 5.0 Receiver Tests

The MIPI Alliance, with the latest introduction of M-PHY® v5.0, provides the ability to connect the latest generation of flash memory-based storage in advanced 5G smartphones and in automotive and computing technologies.

The M-PHY® v5.0 interface introduces a fifth gear (HS-G5), offering a bandwidth of 23.32 Gigabits per second (Gbps), which enables the ecosystem to double the data rate per lane compared with the previous specification.

Calibrations

N5991MM5A fully automates the complex calibration procedure described in the Conformance Test Suite for MIPI M-PHY® v5.0 to generate the stress signal by finely adjusting the pattern generator differential voltage, transmitter equalization, random jitter and periodic jitter at different frequencies to obtain a certain eye opening. In addition, the application gives you clear guidance on how to connect the generator outputs to the oscilloscope for the selected calibration.

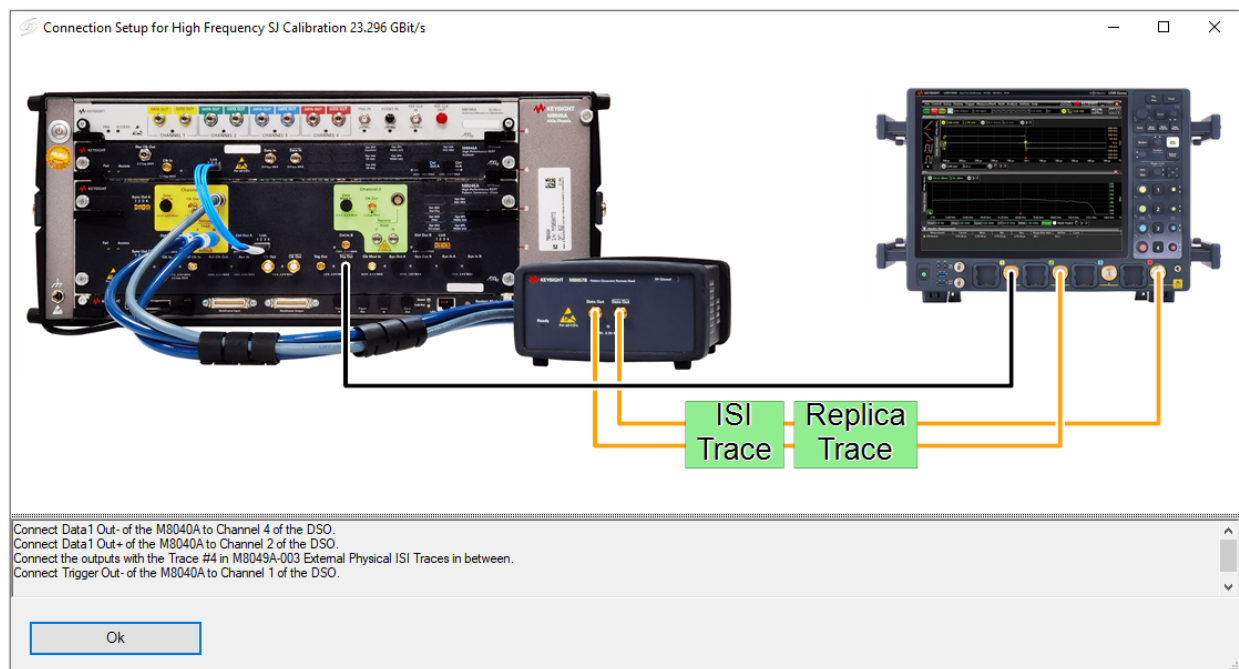


Figure 3. Example connection diagram for High Frequency SJ Calibration

Receiver Tests

The MIPI M-PHY® v5.0 Conformance Test Suite (CTS) defines test procedures for transmitter, receiver and impedance/return loss testing. The tests are designed to determine if a product conforms to specifications defined in the MIPI Alliance Specification for M-PHY®. Successful completion of all tests contained in the suite, combined with a satisfactory level of interoperability testing, will provide a reasonable level of confidence that the DUT will function properly in many environments. Section 2 of the CTS contains the tests that verify various RX signaling voltage, timing and behavioral requirements of M-PHY® transceivers. The N5991MM5A application implements all test procedures defined in the CTS for MIPI M-PHY® v5.0. The user can choose parameters such as HS Gears, default timings, and levels or test pattern sequences that meet the DUT requirements. When in Expert Mode, the application allows testing of the DUT beyond the requirements of the CTS.

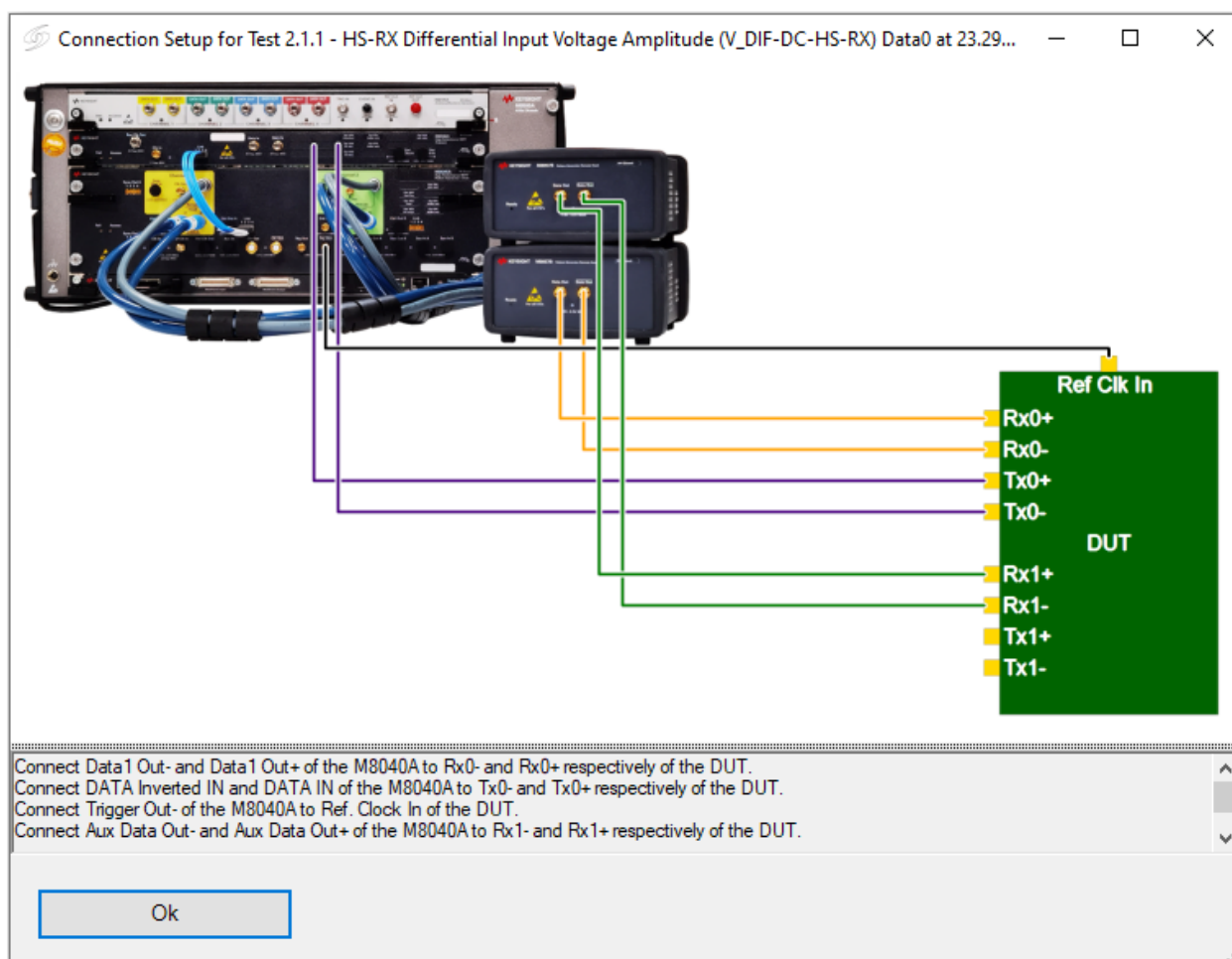


Figure 4. Example connection diagram for Test 2.1.1 - HS-RX Differential Input Voltage Amplitude

Add-ons

UniPro & UFS Support, Add-on

The UniPro protocol provides a transport layer for applications using the M-PHY® interface. Currently it is primarily used by UFS storage devices within mobile phones or tablets. For UniPro and UFS Phy testing, the BERT equipment can be combined with the BIT-3000 DSGA to put the DUT into UniPro Test Mode and retrieve the Frame and Error Counters.

Loop-back Support, Add-on

The DUT is configured in Loop-back Mode, so it will loop back the received test pattern. The M8046 Error Detector (ED) compares the pattern returned by the DUT with the generated pattern to detect if there are bit errors and then computes the Bit Error Ratio. The pattern must match and be in phase. This is ensured by a common reference clock or sharing an explicit clock source. The same pattern is loaded to the BERT pattern generators and the Error Detector. And following CTS to set the right CDR loop bandwidth by HS-Gear when testing. The same pattern is loaded to the generators and the ED. For Loop-back Mode, the M8046A module can be used for error analysis in conjunction with the M8045A pattern generator for the Error Detector.

Integrated BER Counter Interface, Add-on

This option enables the custom BER reader to enable fully automated testing for all transmission modes (HS and LP). This method requires you to implement a class supporting the IBerReader interface, providing access to the DUT's pass/fail information.

Test Coverage

UniPro and M-PHY Lookback Mode

Test ID	Descriptions
HS Tests	
Test 2.1.1	HS-RX Differential DC Input Voltage Amplitude Tolerance
Test 2.1.2	HS-RX Accumulated Differential Input Voltage Tolerance
Test 2.1.3	HS-RX Common-Mode Input Voltage Tolerance
Test 2.1.4	HS-RX Differential Termination Enable Time
Test 2.1.5	HS-RX Differential Termination Disable Time
Test 2.1.6	HS-RX Lane-to-Lane Skew (UniPro only)
Test 2.1.7	HS-RX Receiver Jitter Tolerance
Test 2.1.8	HS-RX Prepare Length Capability Verification
Test 2.1.9	HS-RX Sync Length Capability Verification
Squelch Tests	
Test 2.4.3	SQ-RX Squelch Exit Voltage
Test 2.4.4	SQ-RX Squelch Exit Time
Test 2.4.5	SQ-RX Squelch Noise Pulse Width
Test 2.4.6	SQ-RX Squelch Noise Pulse Spacing
PWM Tests – Non-Terminated Tests	
Test 2.2.1	PWM-RX Differential DC Input Voltage Amplitude Tolerance
Test 2.2.2	PWM-RX Common-Mode Input Voltage Tolerance
Test 2.2.5a	PWM-RX Receive Bit Duration Tolerance
Test 2.2.5b	PWM-RX Receive Bit Duration Tolerance, During LINE-READ
Test 2.2.6	PWM-RX Receive Ratio for PWM-G1
PWM Tests – Terminated Tests	
Test 2.2.1	PWM-RX Differential DC Input Voltage Amplitude Tolerance
Test 2.2.2	PWM-RX Common-Mode Input Voltage Tolerance
Test 2.2.3	PWM-RX Differential Termination Enable Time
Test 2.2.4	PWM-RX Differential Termination Disable Time
Test 2.2.5a	PWM-RX Receive Bit Duration Tolerance
Test 2.2.5b	PWM-RX Receive Bit Duration Tolerance, During LINE-READ
Test 2.2.6	PWM-RX Receive Ratio for PWM-G1
Interference Tests	
Test 2.4.7	SQ-RX Squelch RF Interference Tolerance
Expert Mode only	Common Mode Interference

UFS Mode

Test ID	Descriptions
HS Tests	
Test 2.1.1/3	HS-RX Amplitude and Offset Tolerance
Test 2.1.7	HS-RX Receiver Jitter Tolerance – Positive Offset
Test 2.1.7	HS-RX Receiver Jitter Tolerance – Negative Offset
PWM Tests – Non-Terminated Tests	
Test 2.2.6	PWM-RX Receive Ratio for PWM-G1

N5991MM5E M-PHY 5.0 Frame Generator Software Tool

The Keysight N5991MM5E M-PHY® receiver Frame Generator software maximizes the value of your Keysight M8040A BERT platform, helping you generate signal sequences to test and debug your M-PHY® v5.0 receiver designs easily with an intuitive user interface. The software allows for easy definition of M-PHY data sequences and test patterns, and allows for easy control over all timing, amplitude, and jitter parameters as specified by the MIPI M-PHY® v5.0 specification.

Details:

- Generate custom M-PHY packet sequences and test patterns at HS-GEAR5 (24Gbps) and lower speeds
- Generate custom PWM signal sequences
- Specify and control packet sequence timings
- Specify and control HS timing parameters (PREPARE, STALL, ADAPT)
- Specify and control LS timing parameters
- Specify and control jitter parameters (SJ, RJ)
- Specify and control HS differential and common-mode voltage amplitude parameters

An example connection diagram of the M8040A instrument combined with the BIT-3000 DSGA (used with the N5991MM5E software) is shown in Figure 5.

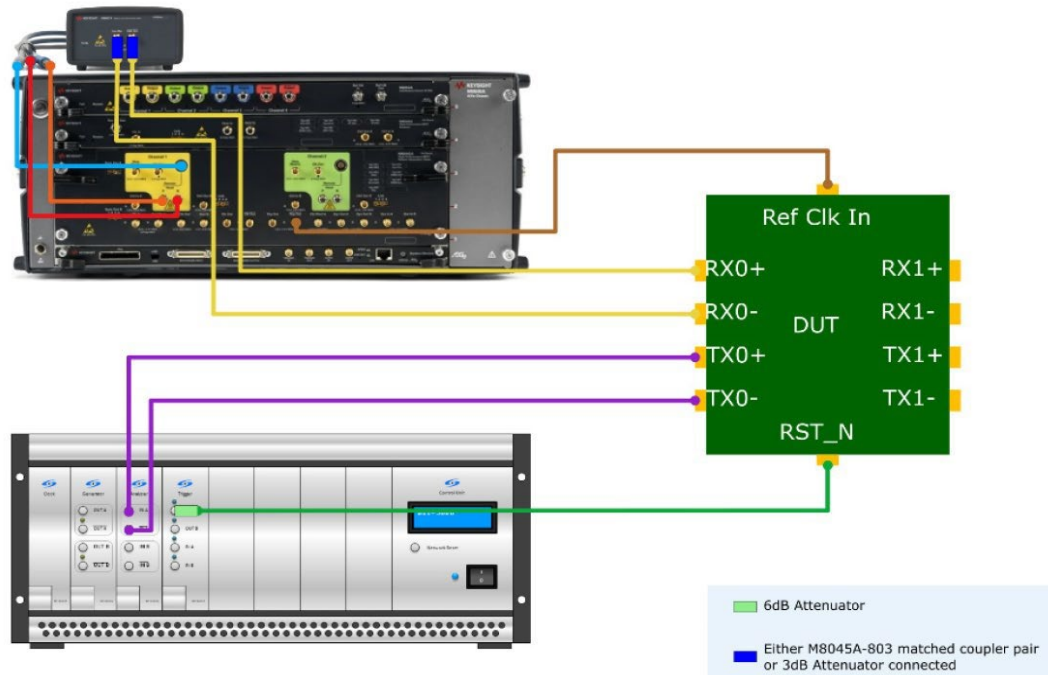


Figure 5. Example connection diagram of M8040A instrument combined with BIT-3000 DSGA

N5991MM5E Features and Layout

The screenshots below summarize the various parameters that the N5991MM5E GUI supports.

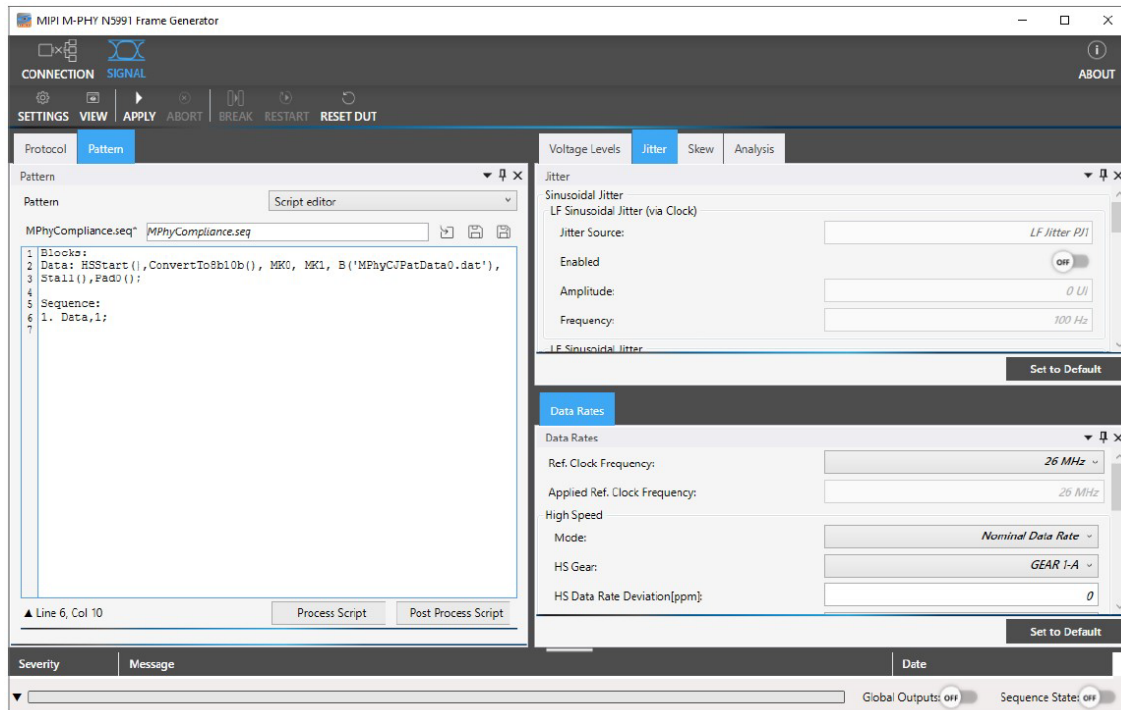


Figure 6. Example of Signal Pattern and Jitter settings

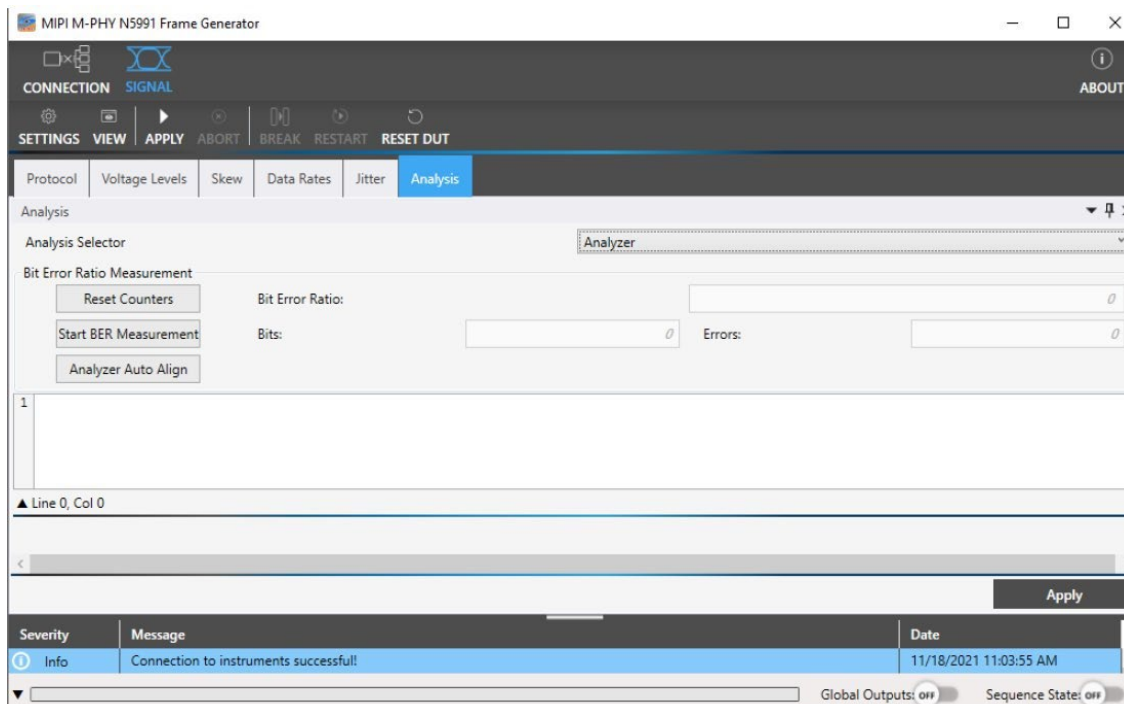


Figure 7. Example of Signal Analysis settings

Recommended Instrument Configurations for MIPI M-PHY 5.0 Receiver Solution

The following equipment are required for use with both N5991MM5A & N5991MM5E. Exact configuration depends on several factors (number of Lanes, error detection method, etc.), which may differ depending on the type of devices being tested.

For full details, please contact Keysight Technologies.

N5991MM5A & N5991MM5E Required Equipment Configuration

UXR Infiniium Oscilloscope (4-channel)	50 GHz and above
M8040A High-Performance BERT with options:	M8040A
Five slot AXIe chassis with embedded controller	M8040A-BU2
M8045A Pattern Generator with options:	M8045A
32 Gbaud or 64 Gbaud NRZ	M8045A-G32 or M8045A-G64
Advanced Jitter Sources for RX Characterization	M8045A-0G3
De-emphasis	M8045A-0G4
Reference Clock Multiplier	M8045A-0G6
M8057B Remote Head for M8045A Pattern Generator	M8057B-FG
M8046A Error Detector with options:	M8046A
32 Gbaud or 64 Gbaud NRZ	M8046A-A32 or M8046A-A64
Clock Recovery up to 32 Gbaud	M8046A-0A4
Interference Source	M8054A
Broadband Coupler Pair, 40 GHz, 2.4mm	M8045A-803
DSGA (BIT-3000) configurations:	
BIT-4000-3000-1 Mainframe	Support UniPro/UFS Rx testing configuration.
BIT-4000-3001-1 Clock Module	
BIT-4000-3003-1 Analyzer Module	
BIT-4000-3004-1 Trigger Module	
BIT-4000-3002-1 Generator Module	Support config DUT to Tx testing mode in UniPro/UFS method.

NOTE: Configuration with M8020A BERT is also available but only enable tests up to Gear 4 for N5991MM5A, not for N5991MM5E.

Ordering Information of Software Products for MIPI M-PHY 5.0 Receiver Solution

M-PHY 5.0 receiver test software products

N5991MM5A	M-PHY 5.0 Receiver Tests
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M-PHY 5.0 debug tools / frame generator software products

N5991MM5E	M-PHY 5.0 Frame Generator
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Licensing options for receiver test and frame generator products

1FP	FP Perpetual node-locked license
1TP	1TP Perpetual transportable single license
SFM	SW maintenance, 1-year, for -1FP license
STM	SW maintenance, 1-year, for -1TP license
SF3	SW maintenance, 3-years, for -1FP license
ST3	SW maintenance, 3-years, for -1TP license

N5991MM5A & N5991MM5E Required Equipment Configuration

N5991MMIY-ADD*	Integrated BER Counter Interface, Add-on
N5991MMUY-ADD*	UniPro & UFS Support, Add-on
N5991MMLY-ADD*	Loop-Back Support, Add-on

NOTE: All add-ons are Transportable license type.

System Requirements

Software

- OS: Windows 10
- Microsoft .NET
- Keysight IO Libraries Suite
- Microsoft Office Excel

NOTE: The exact versions of software requirements are listed in the respective Changelog file and Release Notes.

Hardware

- Connectivity hardware for instrumentation, depending on configuration, e.g., Ethernet
- Multicore processor with 12 logical processors or more
- 16GB RAM or higher

Application Programming Interface (API)

The N5991 ValiFrame API allows ValiFrame functionality (such as test setup information, calibration, and test procedures, and also results) to be accessed from external programming environments. The API does not need a special license to be used. It is included in the base product of a particular standards. The API can thus be used to control the N5991 with external software.

In typical use, a top-level external test sequencer takes advantage of ValiFrame functionality.

Software Maintenance (SWM)

The purchase of one -SFM maintenance license for -1FP product licenses or one -STM maintenance license for -1TP product licenses provides the ability to install updates for one year.

A software maintenance license is always valid for the respective RX test or Debug Tool / Link Training Suite or Frame Generator product only.

Software Maintenance includes updates to newer instrument firmware as well as procedure and test limit changes for the test specifications covered by the products the software maintenance license belongs to. Upgrades to a different test specification are not covered.

All N5991 RX test or Debug Tool / Link Training Suite licenses which were purchased after November 30, 2020 will no longer include automatic Software Maintenance during the first year. Thus, the appropriate software maintenance license is required in order to be able to install updates.

Products that do not have a software maintenance license and are not an Add-on will not be updated but are still operational.

Software without any extra software maintenance product associated with it will have a maintenance expiration date of the license issue date + 14 days as a starting point. The software itself will still work even if the maintenance has expired. If software maintenance has expired, a new software maintenance license can be purchased for this product. However, the new software maintenance will not grant coverage starting from the purchase date but from the date the previous software maintenance coverage expired. For example, if the software maintenance expired on April 30th, 2020 and a new one-year software maintenance was purchased on August 1, 2020, the purchased coverage would begin on May 1, 2020 and would end on April 30, 2021.

Related Products

The **N5991MC2A MIPI C-PHY Receiver Conformance Test Software** covers MIPI C-PHY Receiver conformance testing.

Automated transmitter compliance test is available. **D9050MPHC MIPI M-PHY v5.0 Compliance Test Software for Infiniium Oscilloscope** covers MIPI M-PHY® testing based on v5.0 specification and CTS.

The **UXR-Series oscilloscope** required for testing MIPI M-PHY® v5.0 specification and CTS.

The **M8040A 64 Gbaud High-performance BERT** is currently the only BERT system capable of supporting MIPI M-PHY® v5.0 specification and CTS Receiver test requirements.

The **M8020A J-BERT High-Performance BERTs** provide Receiver testing capabilities up to MIPI M-PHY® v4.0 specification and CTS.

The **M8070B System Software** is the main software for M8000 Series of BER Test Solutions.

The **MIPI M-PHY v5.0 Interface S-Parameter and Impedance Test MOI** is a guide for Tx/Rx Hot TDR Compliance Tests using Keysight's Vector Network Analyzer (E5080B).