Type-C接口在HDMI和DisplayPort等显示标准中的应用和测试

Apr. 20th, 2017

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KEYSIGHT TECHNOLOGIES

Agenda

- Type-C 简介
- HDMI1.4b over Type-C
- DP over Type-C
- 阻抗和Type-C电缆测试介绍
- Final Words

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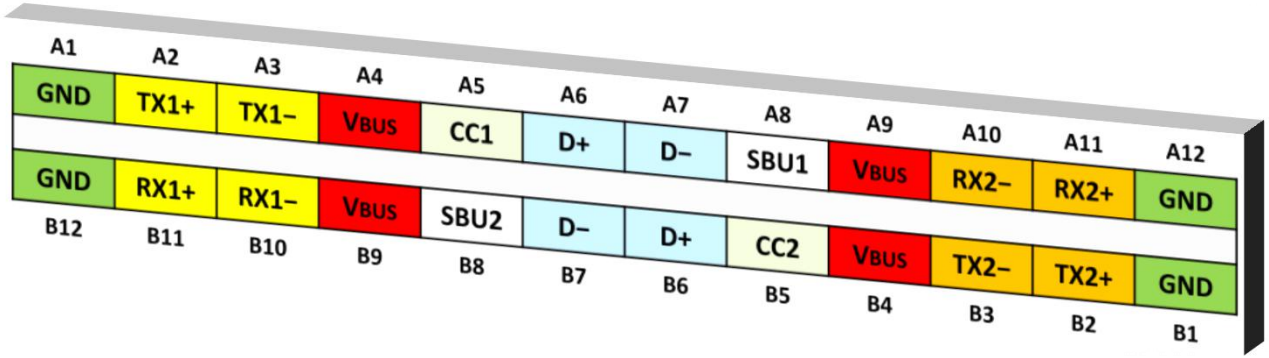
Industry Drivers for Type-C™

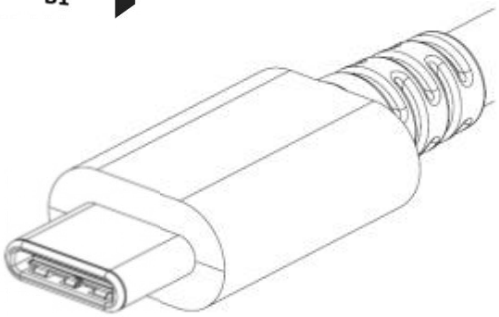
- ★ *支持正反插，不受方向性约束*
- ★ *Alternate Mode，支持以其他标准协议通讯 (DP1.4, TBT, MHL4.0, HDMI…)*
- ★ *制定 power delivery 电力传输和充电机制 (Up to 100 Watts)*

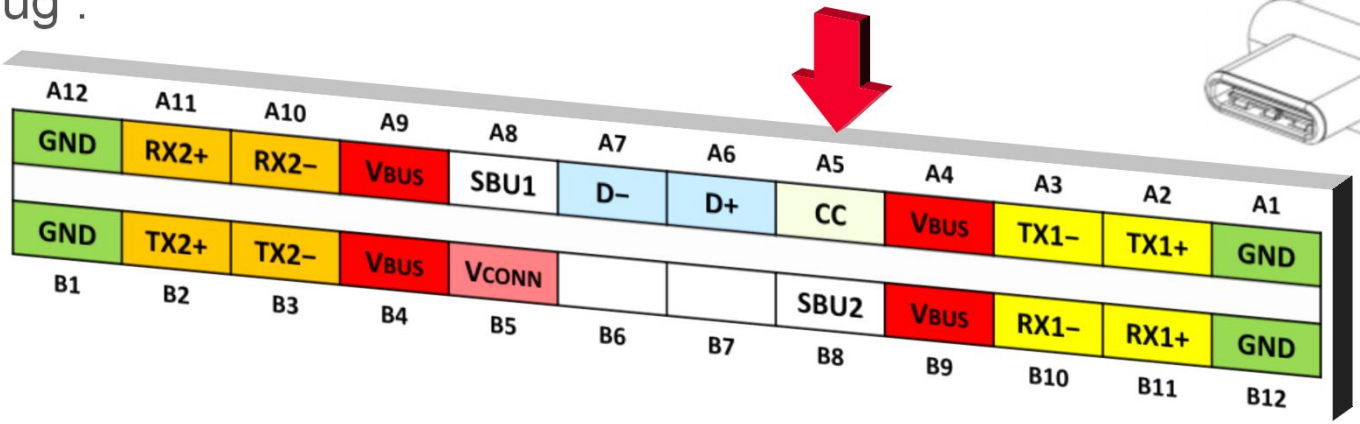
Type-C™ Functional Pin-out

Looking into the product receptacle :



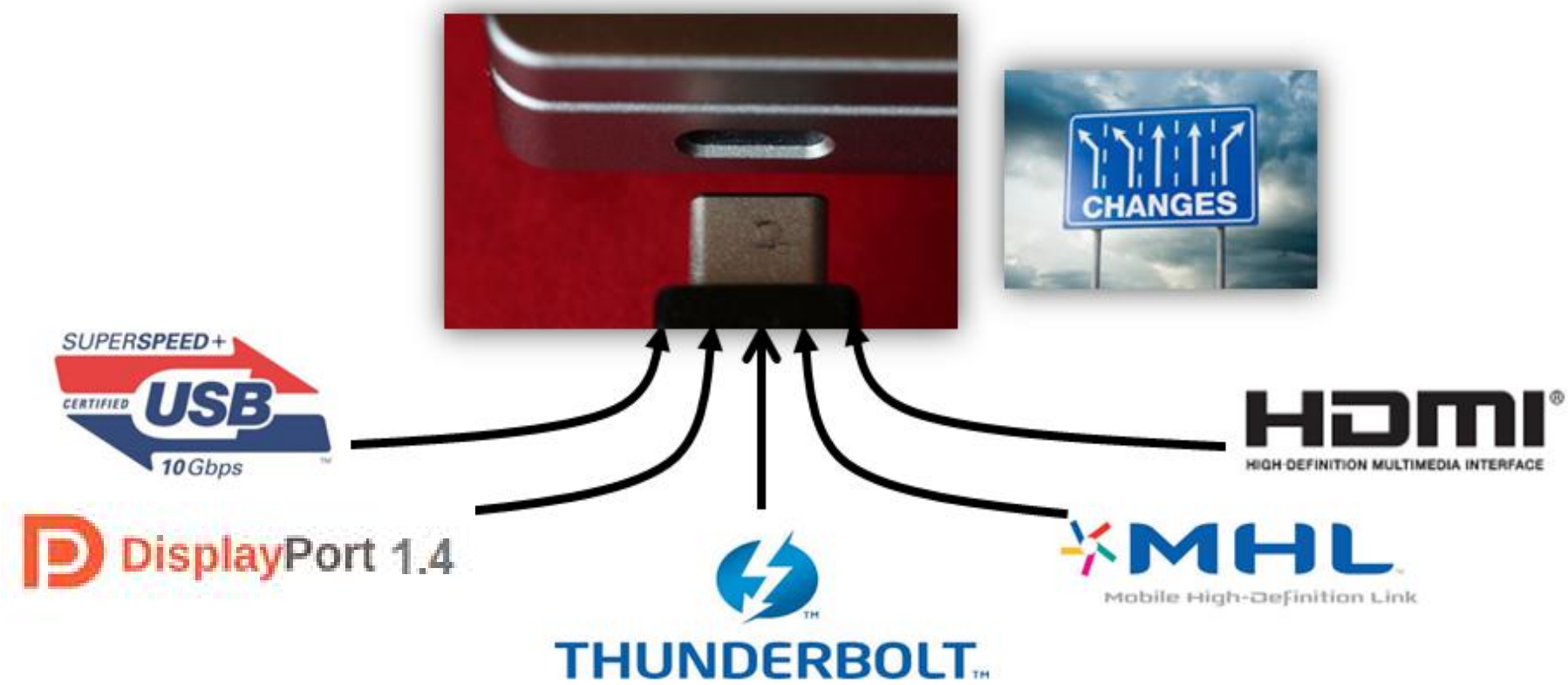
Looking into the cable or product plug :





Type-C™ Alternate Mode

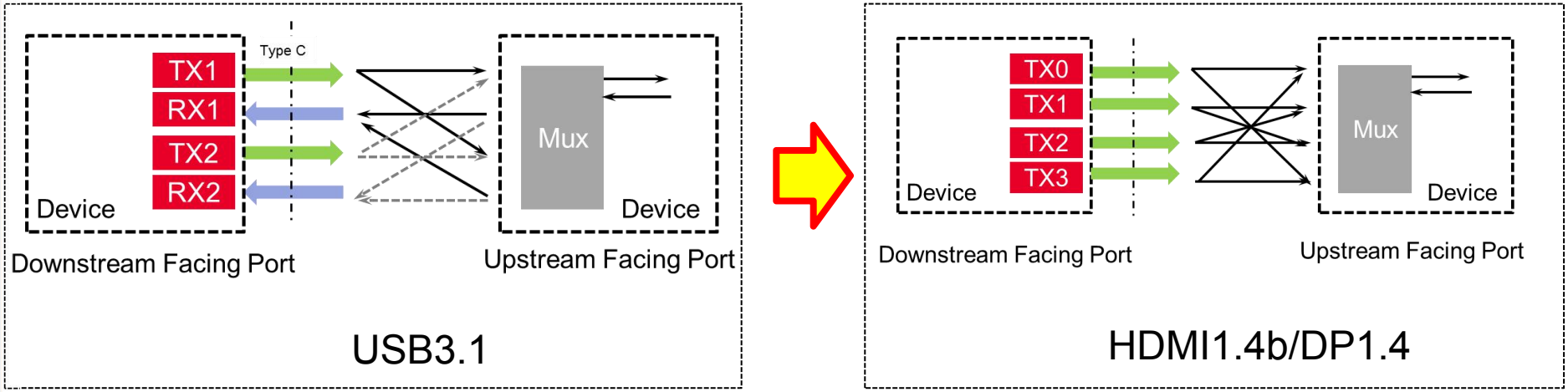
A port could wake up as USB 3.1, then get configured to DisplayPort、HDMI or …



Alternate Mode

– An operational mode of devices on a link that dynamically reassigns USB Type-C pin functionality by communication via the Power Delivery channel to change the character of the link.

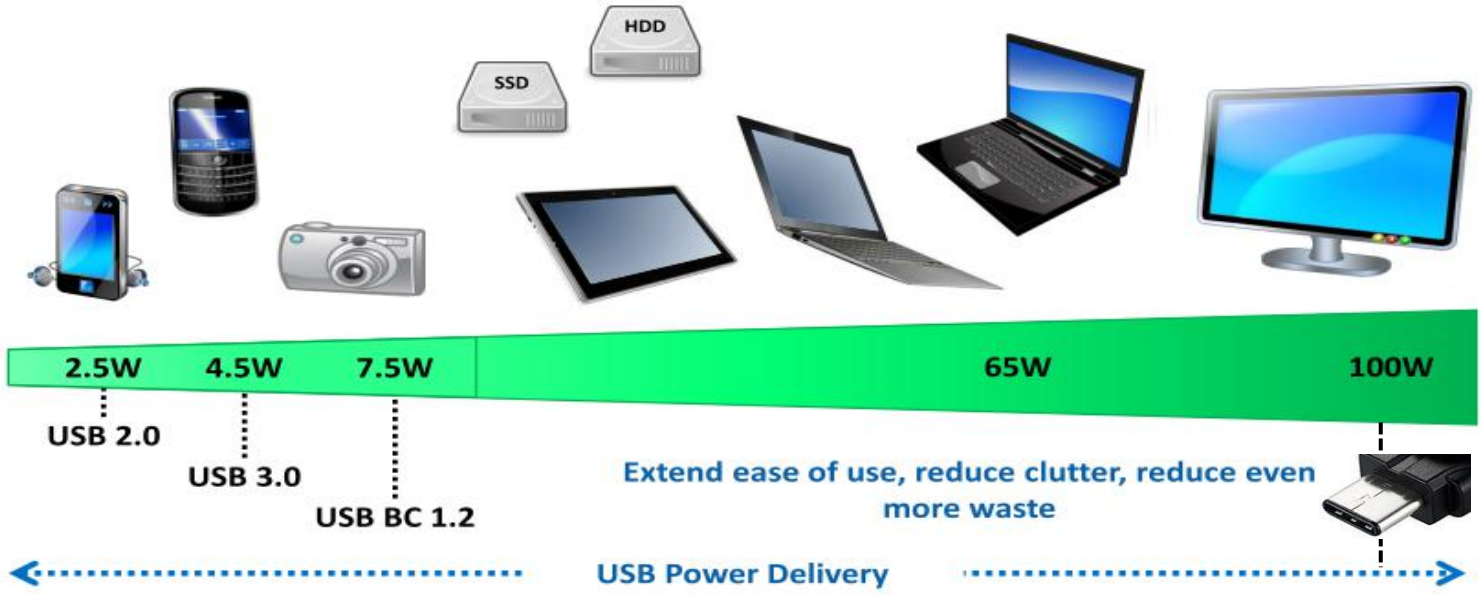
Example: a 'device' can wake up USB3.1 and change to HDMI1.4b/DP1.4



HDMI1.4b,DisplayPort 1.4, MHL, & Thunderbolt

Type-C™ Power Delivery 3.0

CERTIFIED USB CHARGER 45W™



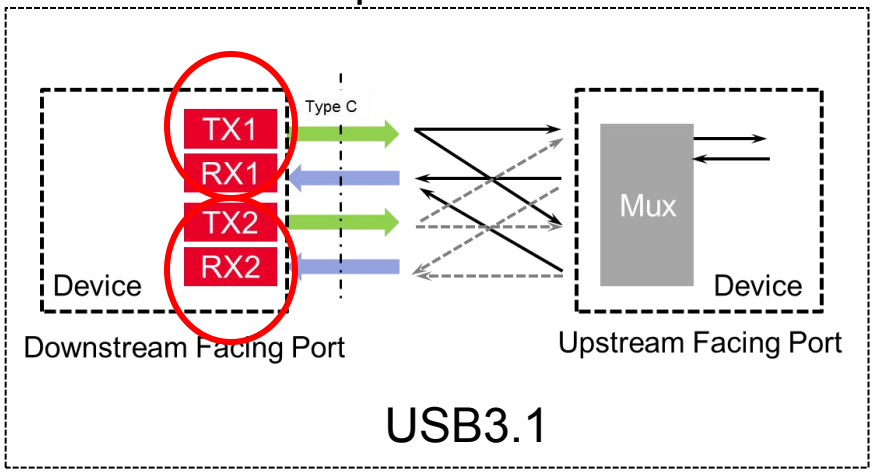
Precedence	Mode of Operation		Nominal Voltage	Maximum Current
Highest	USB PD		Configurable	5 A
	USB Type-C Current @ 3.0 A		5 V	3.0 A
	USB Type-C Current @ 1.5 A		5 V	1.5 A
↓	USB BC 1.2		5 V	Up to 1.5 A
	Default USB Power	USB 3.1	5 V	900 mA
Lowest		USB 2.0	5 V	500 mA

PROFILE 1 5V @ 2A	10W Default
PROFILE 2 5V @ 2A, 12V @ 1.5A	18W
PROFILE 3 5V @ 2A, 12V @ 3A	36W
PROFILE 4 5V @ 2A, 12V, 20V @ 3A	60W Limit fo
PROFILE 5 5V @ 2A, 12V, 20V @ 5A	100W Limit fo

Sink/source can be swapped, power direction no longer fixed

Type C Testing Challenge

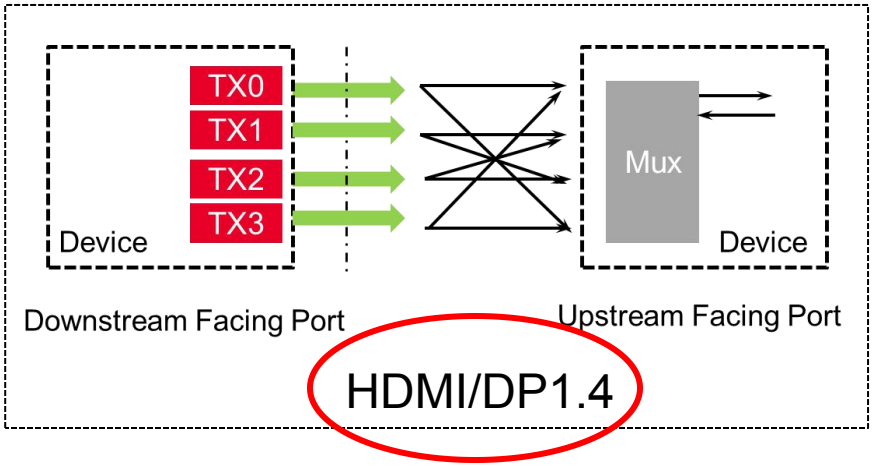
Orientation Independence



Test time DOUBLES

Test Twice for USB3.1 /2.0

Alternate Mode



Test HDMI/DisplayPort!

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HDMI1.4b over Type-C

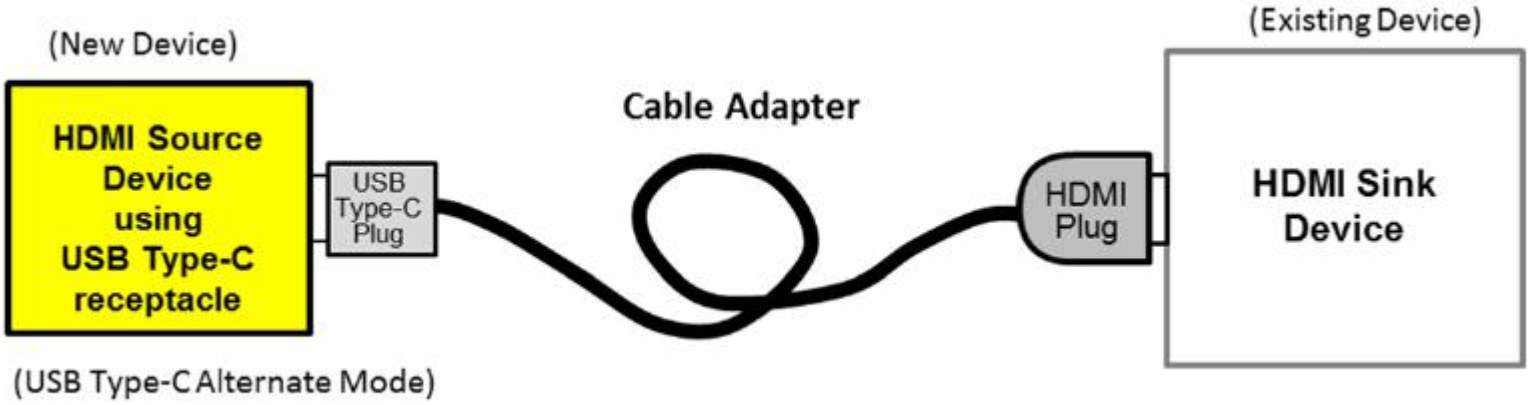


Figure 2: Use case for mapping HDMI to USB Type-C connector

The features:

☆ HDMI Source Device that uses USB Type-Connector as an Alternate Mode.

☆ HDMI Cable Adapter that adapts USB Type-C connector to HDMI connector.

HDMI1.4b over Type-C

☆ USB version

- ◆Universal Serial Bus 3.1 Specification Revision 1.0
- ◆USB Type-C Cable and Connector Specification Revision 1.2 Max Data rate:10GB
- ◆USB Power Delivery Specification Revision 2.0

  Max Power:100W

☆ HDMI version

- ◆High Definition Multimedia Interface Specification Version 1.4b

  Max Data rate:10.2GB
- ◆HDMI Compliance Test Specification Version 1.4b

HDMI1.4b over Type-C

Table 1: HDMI Source Pin Assignment for USB Type-C connector

Pin	Rev Pin	Description	HDMI Function	Pin	Rev Pin	Description	HDMI Function
A1	B1	Common Ground	TMDS Data 1 Shield	B12	A12	Common Ground	TMDS Data 2 Shield
A2	B2	Switched with TMDS Clock-	TMDS Data 1+	B11	A11	Switched with TMDS Data 0-	TMDS Data 2+
A3	B3	Switched with TMDS Clock+	TMDS Data 1-	B10	A10	Switched with TMDS Data 0+	TMDS Data 2-
A4	B4	VBUS (USB Type-C)		B9	A9	VBUS (USB Type-C)	
A5	B5	Integrated on CC signaling	CEC SCL/SDA	B8	A8	Switched with HPD/HEAC-	Utility/ HEAC+
A6	B6	D+ (USB Type-C)		B7	A7	D- (USB Type-C)	
A7	B7	D- (USB Type-C)		B6	A6	D+ (USB Type-C)	
A8	B8	Switched with Utility/HEAC+	HPD/ HEAC-	B5	A5	V_{CONN} (+5V Power)	+5V Power
A9	B9	VBUS (USB Type-C)		B4	A4	VBUS (USB Type-C)	
A10	B10	Switched with TMDS Data 2-	TMDS Data 0+	B3	A3	Switched with TMDS Data 1-	TMDS Clock+
A11	B11	Switched with TMDS Data 2+	TMDS Data 0-	B2	A2	Switched with TMDS Data 1+	TMDS Clock-
A12	B12	Common Ground	TMDS Data 0 Shield	B1	A1	Common Ground	TMDS Clock Shield

HDMI1.4b over Type-C

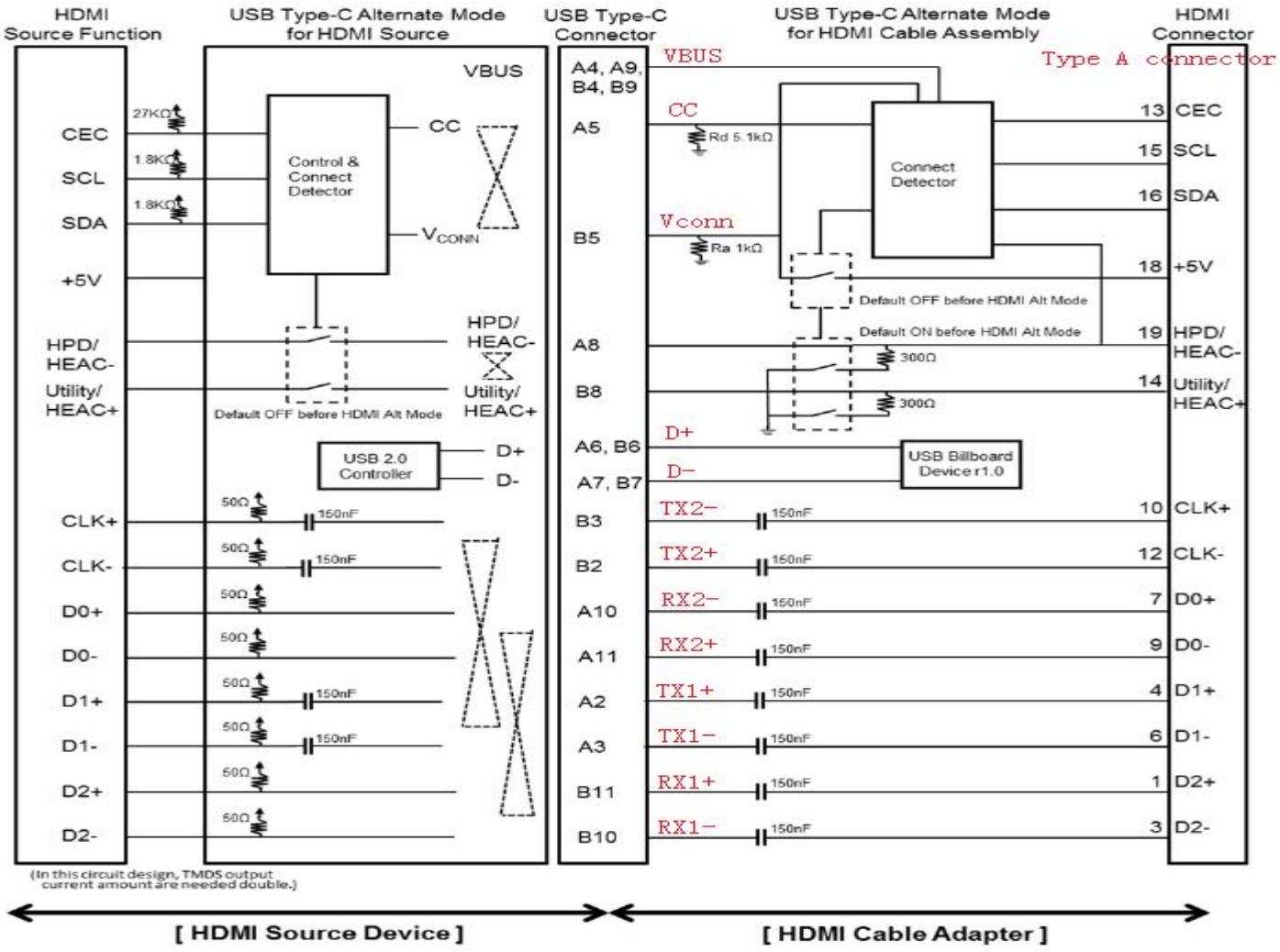


Figure 4: Reference Circuit Design for HDMI Alternate Mode of USB Type-C

HDMI1.4b over Type-C

- VDM Header

Table 9: VDM Header (CEC Write from Source to Cable Adapter)

Bits	Field	Description	
4..0	Command	11h = CEC Write	10001
5	Reserved	0	0
7..6	Command Type	00b = Initiator	00
10..8	Object Position	001b = HDMI Mode	001
12..11	Reserved	00b	00
14..13	SVDM Version	00b = Version 1.0	00
15	VDM Type	1 = Structured	1
31..16	Standard or Vendor ID	HDMI_SID	FF04

VDM Header(CEC Write from Source to Cable Adapter):

FF04 1 00 00 001 00 0 10001 → FF04 1000 0001 0001 0001

FF04 8 1 1 1

VDM Header(CEC Read from Cable Adapter to Source):

FF04 81 12

HDMI1.4b over Type-C

- Example for CEC command format
  - CEC Write Header

Table 10: CEC Write Header

Bits	Field	Description
0	Start Bit	If this is set, the PD-CEC Decoder shall generate a Start bit before transmitting data
1	End of Message	If this is set, the PD-CEC Decoder shall set the EOM bit in the last block
6..2	Effective Data Byte	The number of effective Data Byte in this VDM
31..7	Reserved	This shall be set to 0

HDMI1.4b over Type-C

Table 20: VDM Header (DDC Write)

Bits	Field	Description	
4..0	Command	13h = DDC Write	10011
5	Reserved	0	0
7..6	Command Type	00b = Initiator	00
10..8	Object Position	001b = HDMI Mode	001
12..11	Reserved	00b	00
14..13	SVDM Version	00b = Version 1.0	00
15	VDM Type	1 = Structured	1
31..16	Standard or Vendor ID	HDMI_SID	FF04

VDM Header(DDC Write from Source):

FF04 1000 0001 0001 0011

FF04 8 1 1 3

VDM Header(DDC Read from Source):

FF04 81 14

HDMI1.4b over Type-C

◆Note: The following test shall meet the HDMI specification version 1.4b

6.4 HDMI Cable Assembly test

☆ Cable Electrical test item

HDMI CTS1.4b		Type C Testing Items	Notice
5-1	connector maximum envelope	Yes	
5-2	wire Assignment	SKIP	
5-3	TMDS-Eye Diagram	Yes	
5-4	Intra-Pair skew	Yes	USB Type-C Fixture
5-5	Inter-Pair skew	Yes	
5-6	Far End Crosstalk	Yes	
5-7	Attenuation and Phase	Yes	
5-8	Differential Impedance	Yes	

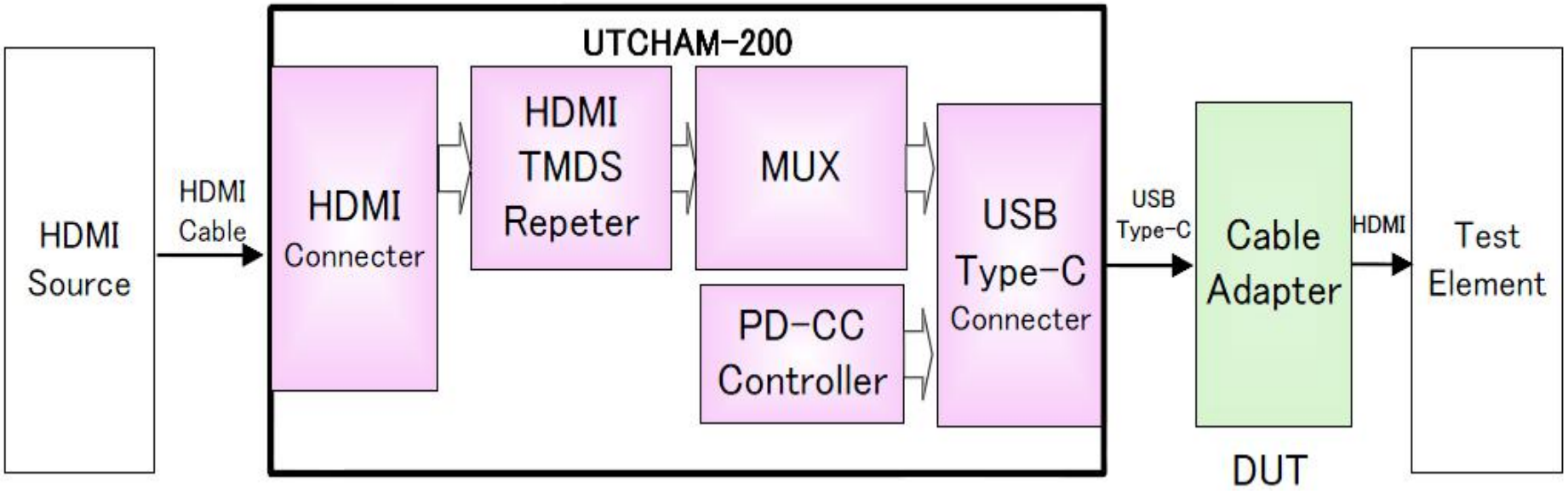
HDMI1.4b over Type-C

◆Test Item

HDMI CTS1.4b		Type C Testing Items	Notice
5-10	DDC/CEC Line Capacitance and Voltage	Yes	Test as "Converter Cable"
5-11	5V Power	Yes	Test as "Converter Cable"
5-12	Hot Plug Detect	Yes	Test as "Converter Cable"
5-13	DDC Communication	Yes	Test as "Converter Cable"
5-14	CEC Communication	Yes	Test as "Converter Cable"
5-15	Utility Line Impedance	Yes	
5-16	Type E cable wire thermal deformation	No	
6-1	HEAC Intra-Pair skew test	Yes	
6-2	Differential Attenuation Test	Yes	
6-3	Differential/Common Impedance Test	Yes	

HDMI1.4b over Type-C

◆Connection Example for USB Type-C HDMI Alt Mode Cable Adapter Control Board and Cable Adapter(DUT):



← Panasonic UTCHAM-200

Used for Test: DDC,HPD,+5V and HDCP

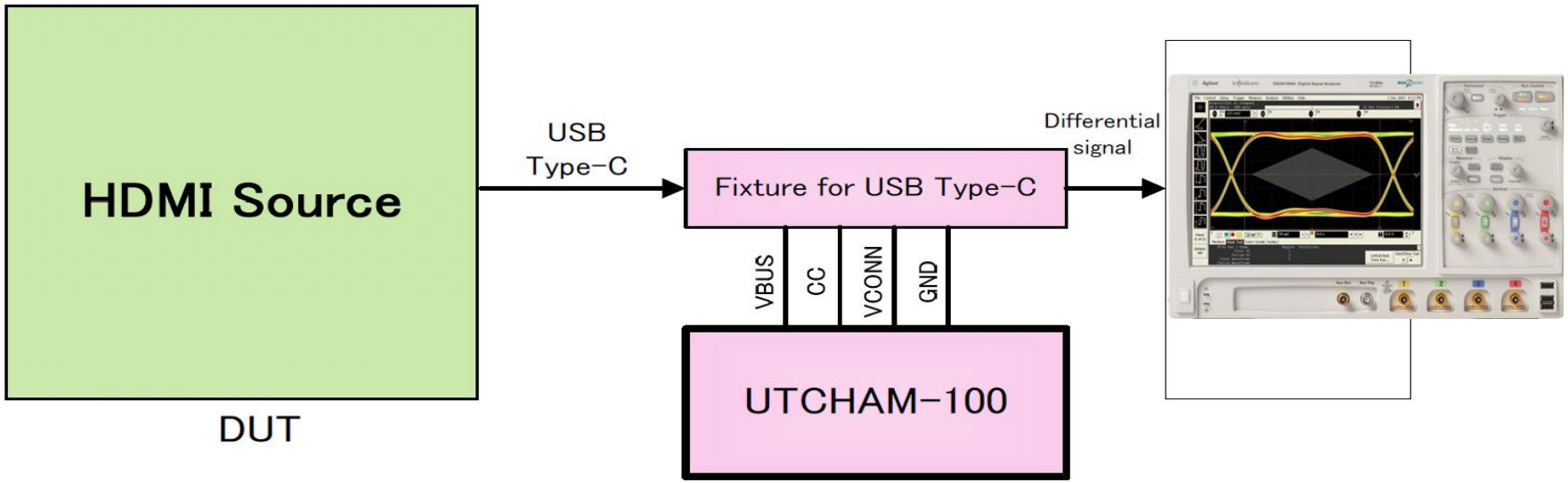
HDMI1.4b over Type-C

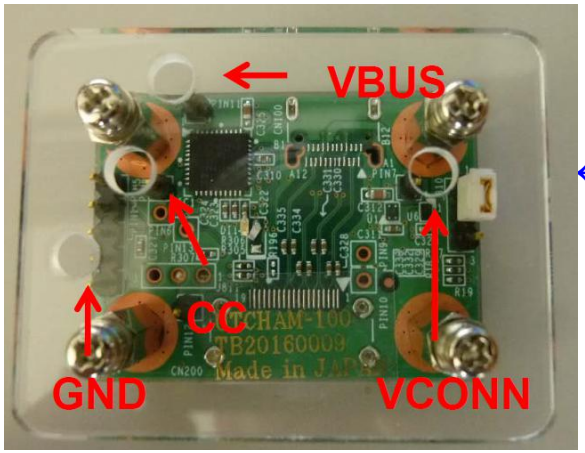
◆Test Item

HDMI CTS1.4b		Type C Testing Items	Notice
7-1	EDID	Yes	
7-2	VL	SKIP	
7-3~7-12		Yes	
7-13	DDC/CEC Capacitance and Voltage	SKIP	
7-14	CEC Line Connectivity	SKIP	
7-15	CEC Line Degradation	SKIP	
7-16~7-40	Protocol	Yes	
HDCP	Protocol	Yes	Using Reference Cable adapter
CEC	Protocol	Yes	Using Reference Cable adapter
HEAC		Yes	Using Reference Cable adapter

HDMI1.4b over Type-C

◆Connection Example for Source Control Board and HDMI Source(DUT):



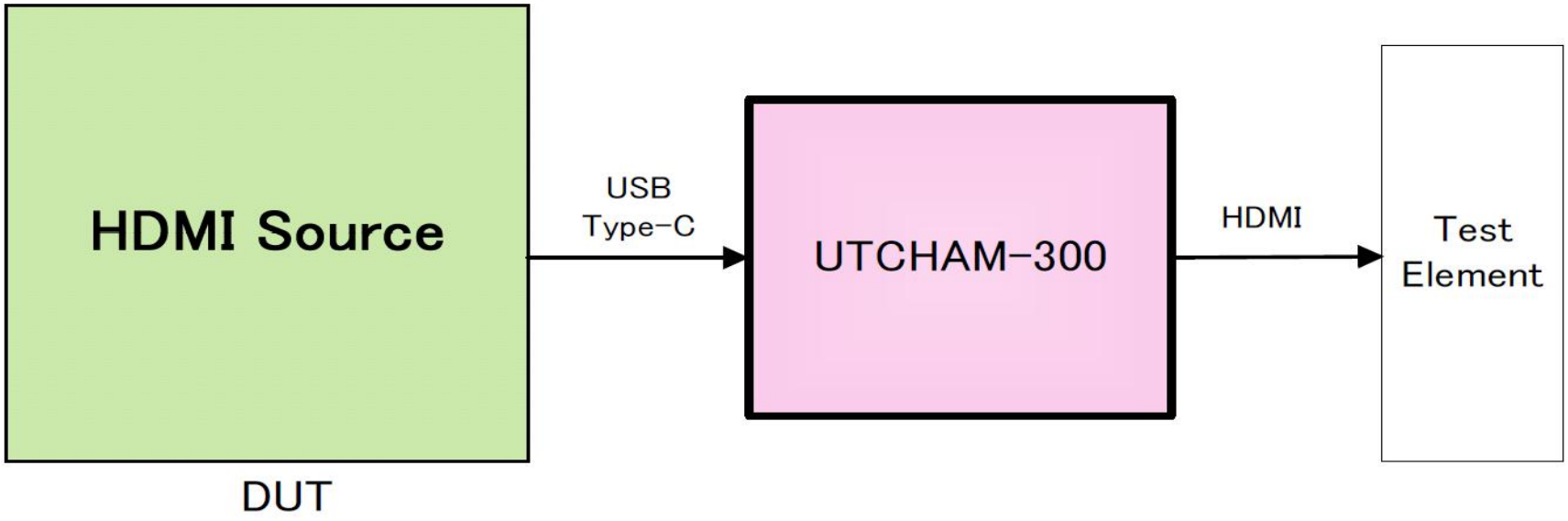


← Panasonic UTCHAM-100

Used for Test: Difference Line Analog test

HDMI1.4b over Type-C

◆Connection Example for USB Type-C HDMI Alt Mode Reference Cable Adapter and HDMI Source(DUT):

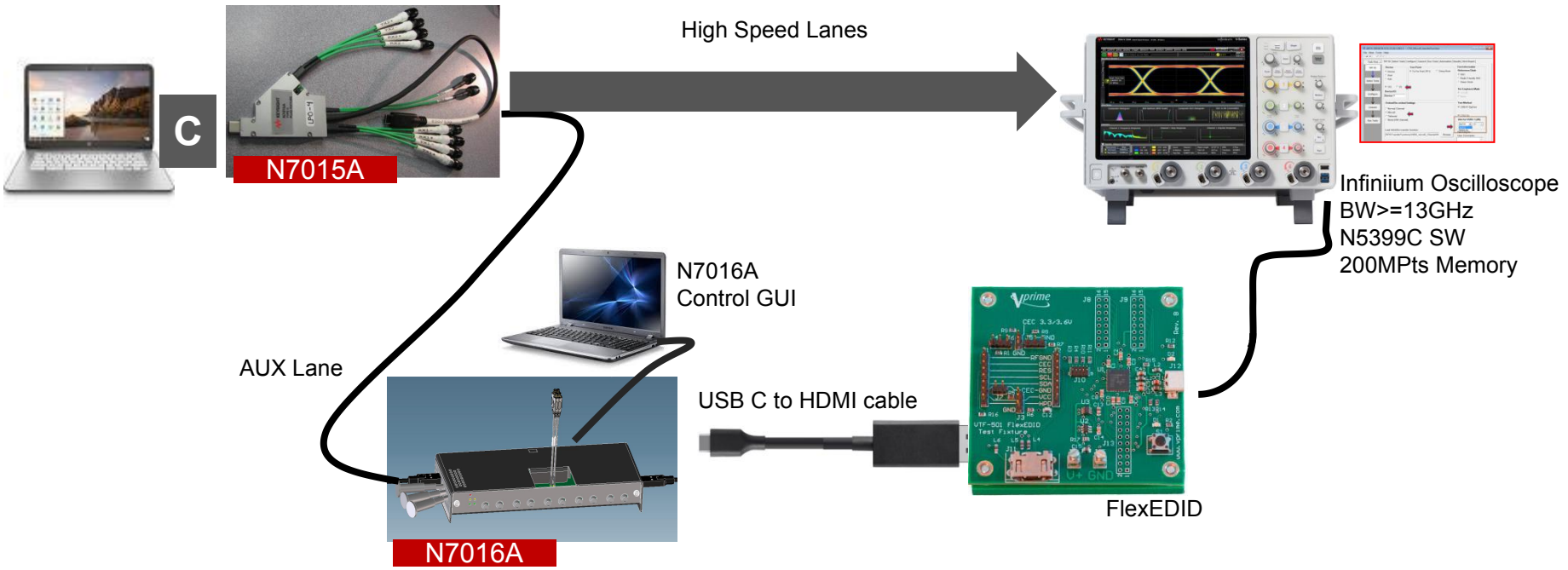


← Panasonic UTCHAM-300

Used for Test: EDID,HDMI Protocol , HDCP Protocol

Keysight HDMI1.4b Type-C TX Solution

Assumptions: Devices require power contract and means to get into alternate mode. RX and TX testing separate.



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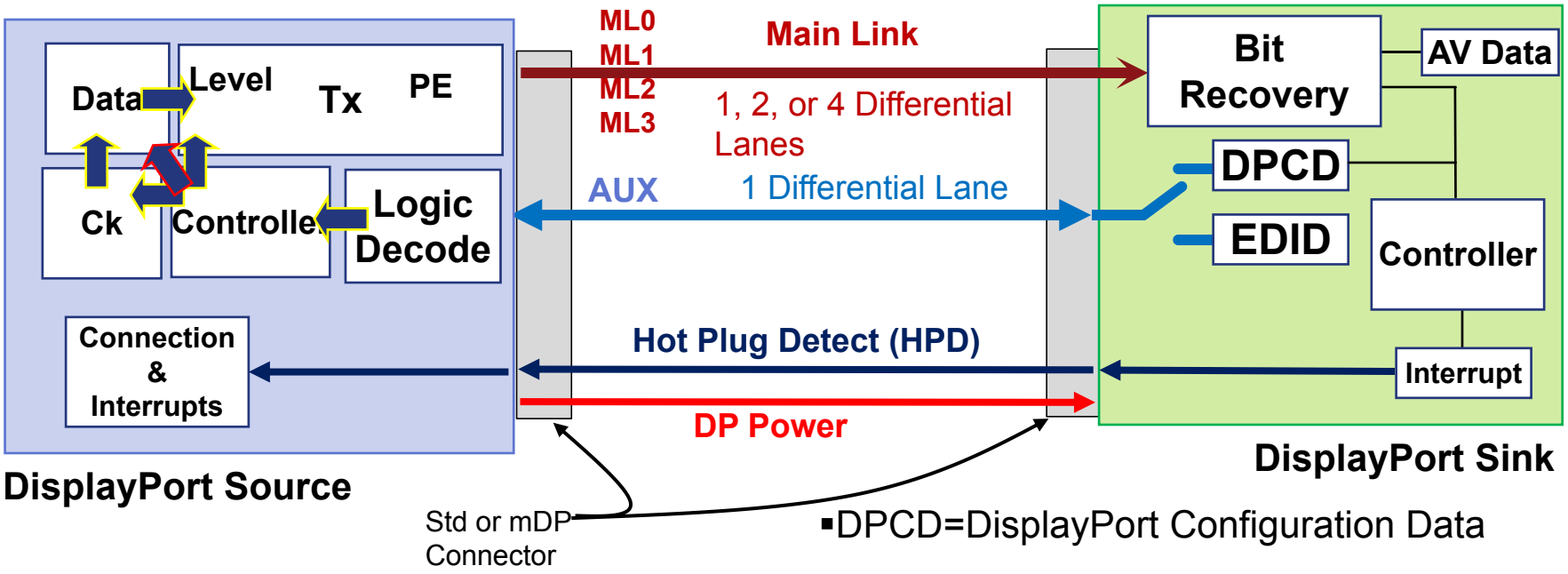
DisplayPort Link review

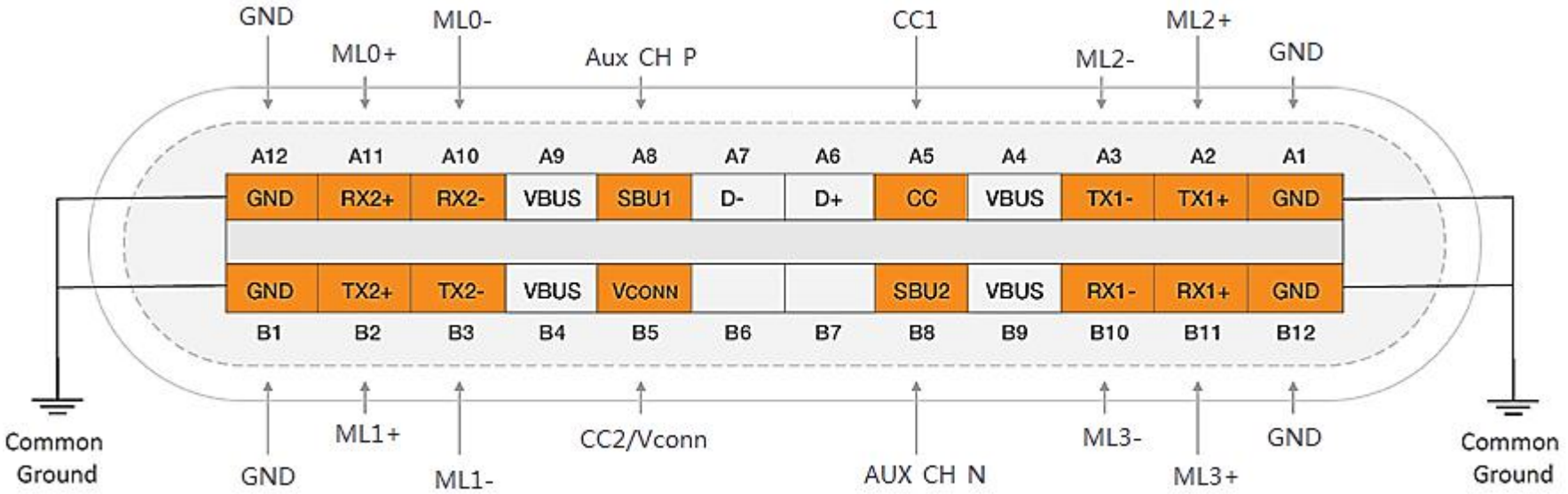


Data rates		Levels
AUX	1Mbs	0: 400mVpp nom
RBR	1.62Gbs	1: 600mVpp nom
HBR	2.7Gbs	2: 800mVpp nom
HBR2	5.4Gbs	3:1200mVpp nom
1.4 HBR3	8.1Gbs	

- DPCD=DisplayPort Configuration Data
- EDID=Extended Display Identification Data
- AUX lines and HPD used to establish connection between the Source and the Sink through the interconnecting channel.
- The DP sink can request service by an interrupt pulse on HPD line .
- Video and Audio sent via packet structure
- Each link partner has own source of power

KEYSIGHT TECHNOLOGIES

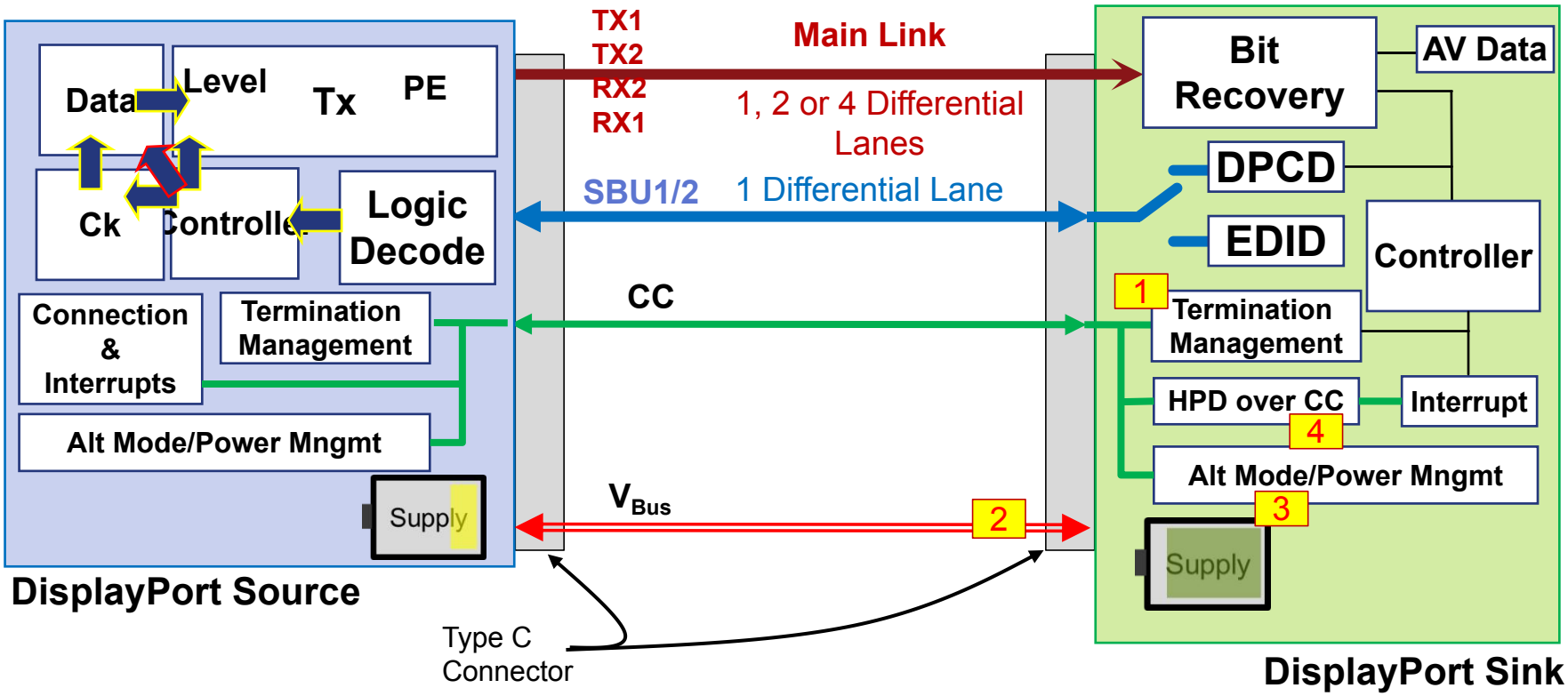
Alt Mode DP over Type-C Pin Assignments



Pin	Signal Name	Alt Mode Signal Name	Description	Pin	Signal Name	Alt Mode Signal Name	Description
A1	GND	GND		B12	GND	GND	
A2	SSTXp1	ML2+	HS Lane	B11	SSRXp1	ML3+	HS Lane
A3	SSTXn1	ML2-	HS Lane	B10	SSRXn1	ML3-	HS Lane
A4	VBUS	VBUS		B9	VBUS	VBUS	
A5	CC1	CC1	Header Pin	B8	SBU2	AUX_CH_N	SMA
A6	Dp1	Dp1	*Optional	B7			NC
A7	Dn1	Dn1	*Optional	B6			NC
A8	SBU1	AUX_CH_P	SMA	B5	CC2	CC2/VCONN	Header Pin
A9	VBUS	VBUS		B4	VBUS	VBUS	
A10	SSRXn2	ML0-	HS Lane	B3	SSTXn2	ML1-	HS Lane
A11	SSRXp2	ML0+	HS Lane	B2	SSTXp2	ML1+	HS Lane
A12	GND	GND		B1	GND	GND	

KEYSIGHT TECHNOLOGIES

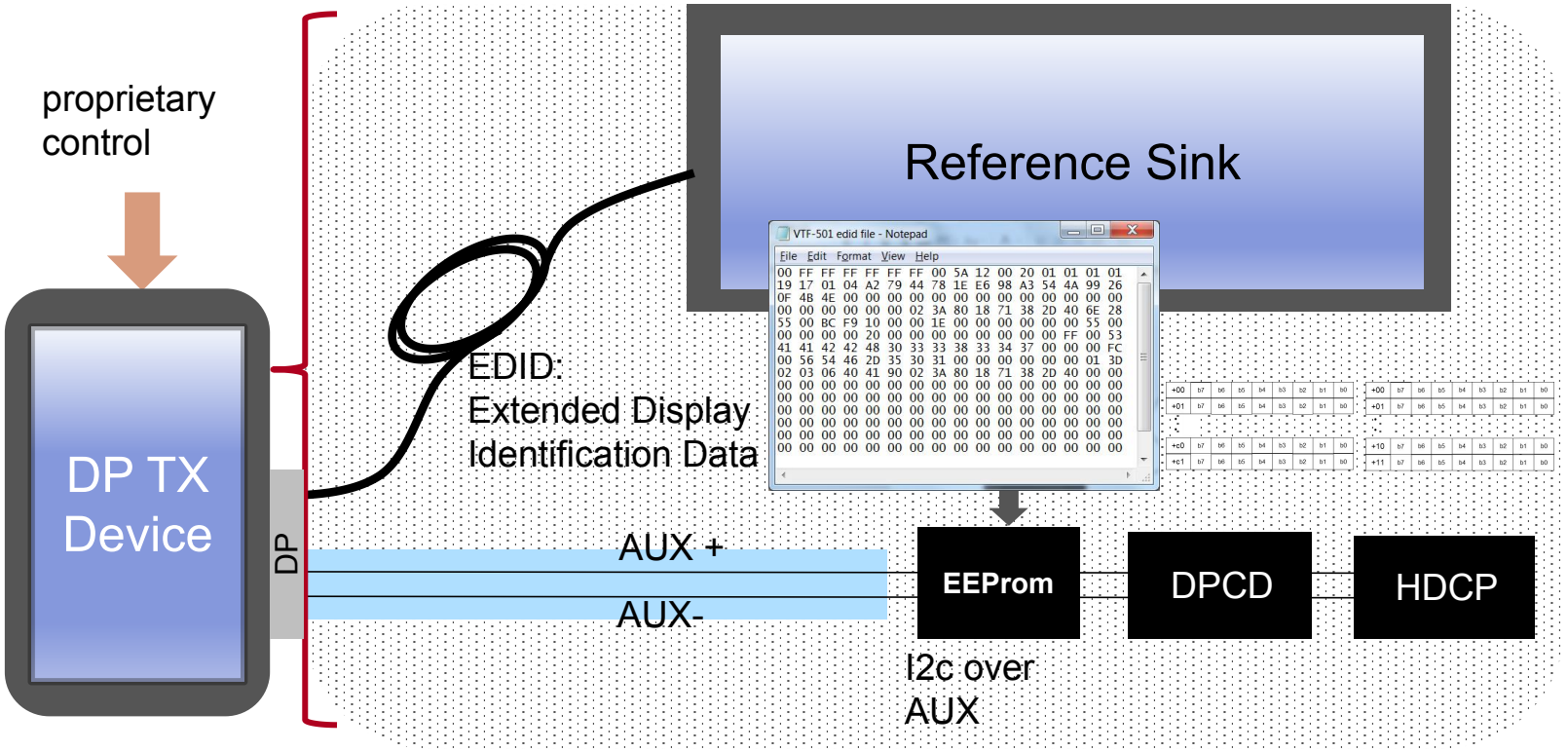
DisplayPort Link over Type-C



New issues brought about because of USB Type-C

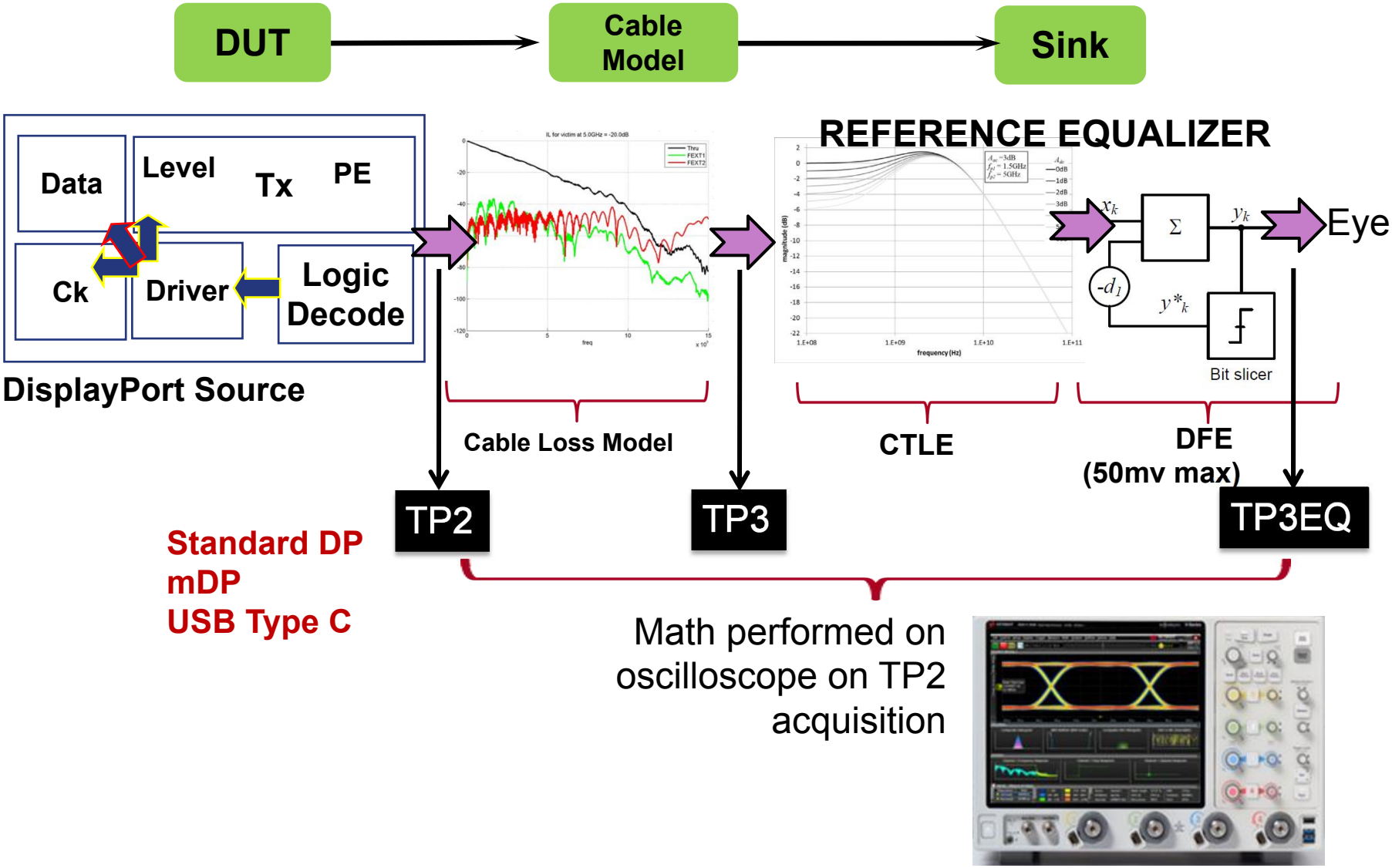
Understanding DisplayPort test

We use a Reference Sink to control DUT



- Sometimes customers have control (proprietary) of their TX device so don't care about control over the AUX lines.
- Device is put into a Test mode using Test mode control through DPCD
- I have never seen an HDCP issue.

DP Transmitter Testing: Whole Channel



DP Source Test Solution element checklist

Solution Element	Description	Comment
Oscilloscope	**Infiniium**	**13GHz minimum**
Scope options	DP U7232D Infiniisim Basic Equalization	Sw app De-embedding and cable embedding Required for DP1.4
Probes	1169A/N5380B N2800A/N5444A N2832A/N5444A N700xA/N5444A N7010A	Optional Not common
Cables	N2823A 1 meter N5448B 10”	
Test Point Adapter	Wilder TPA and aux N7015/16	Std or mDP Type C
Reference sink	DPR-100	
Other	Connector savers or adapters, or cables	For instance for N7010As and matched cables, Or for routing through switch.
Switching SW	U7232D 7FP	Activates the switch control option in N5399C
Switch	Bitifeye 2100D	Most flexible switch box available
Precision Probe	N2809A	For path loss and skew correction

DisplayPort Source Tests: Patterns and Test Point

Test	RBR	HBR	HBR2	HBR3
3-1 Eye Diagram	PRBS7	PRBS7/ CP2520	CP2520 TP3EQ	TPS4 TP3EQ
3-2 Non Pre-Emphasis Level	PRBS7	PRBS7	PRBS7	PRBS7
3-3 Pre-Emphasis Level	PRBS7	PRBS7	PLTPAT	PLTPAT
3-4 Inter Pair Skew	D10.2	D10.2	D10.2	TPS4
3-11 Non ISI Jitter	PRBS7	PRBS7	NA	NA
3-11 Deterministic Jitter	NA	NA/ CP2520	CP2520 TP3EQ	TPS4 TP3EQ
3-12 Total Jitter	PRBS7	PRBS7/ CP2520/D10.2	CP2520/D10.2 TP3EQ	TPS4 TP3EQ
3-14 Main Link Frequency	D10.2	D10.2	D10.2	D10.2
3-15 Spread Spectrum Modulation Frequency	D10.2	D10.2	D10.2	D10.2
3-16 Spread Spectrum Deviation Accuracy	D10.2	D10.2	D10.2	D10.2

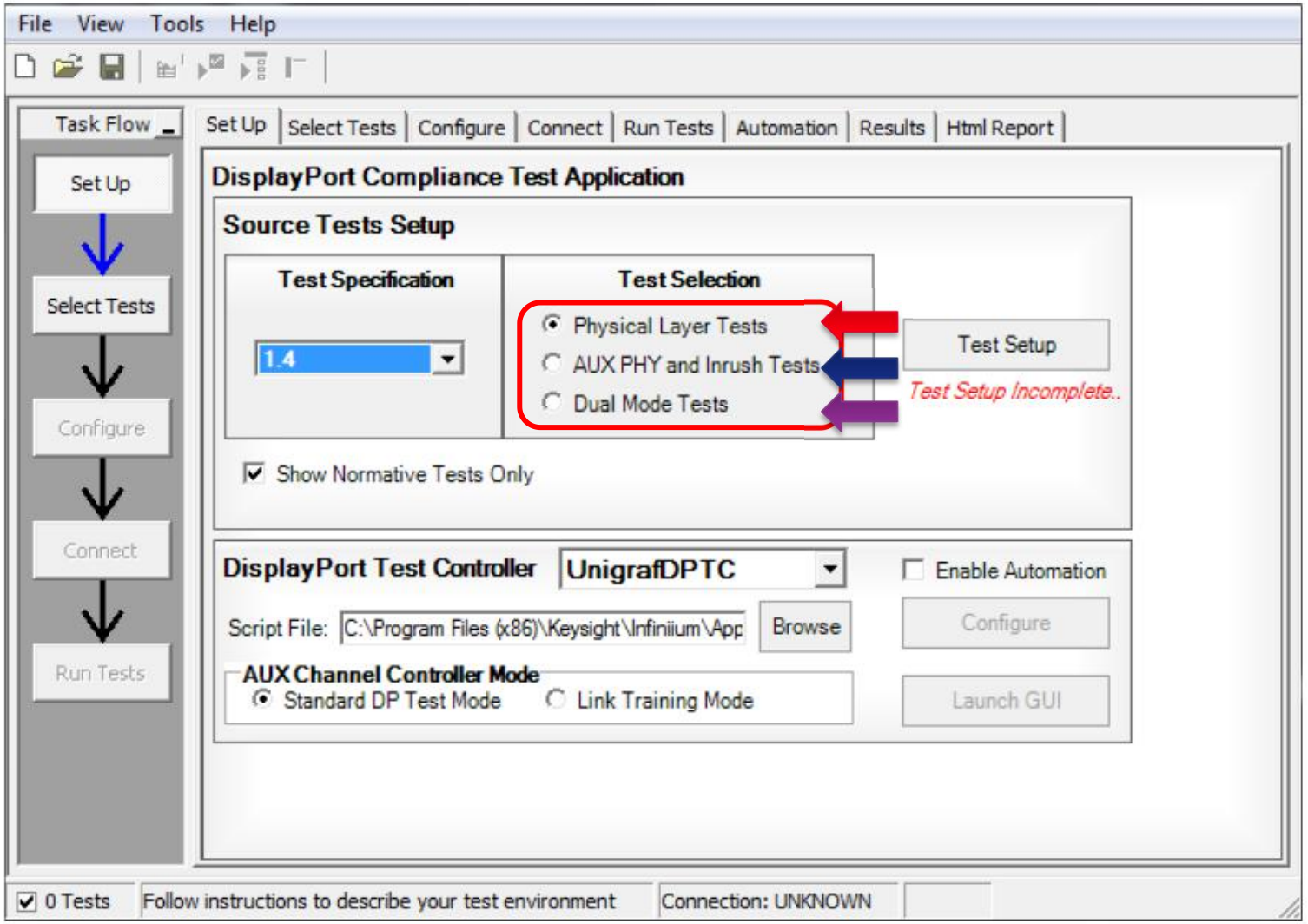
All measurement points are TP2 unless noted

DisplayPort Source Tests and Levels & Pre-Emphasis

Test	Levels	Pre-Emphasis
3-1 Eye Diagram	RBR/HBR: Setting 2 HBR2/3: User Choice	RBR/HBR: Setting 0 HBR2/3: User Choice
3-2 Non Pre-Emphasis Level	All Settings	Setting 0
3-3 Pre-Emphasis Level	All Settings	All Valid Settings
3-4 Inter Pair Skew	Setting 2	Setting 0
3-11 Non ISI Jitter	RBR/HBR: All settings	RBR/HBR: Setting 0
3-11 Deterministic Jitter	RBR/HBR: All settings HBR2/3: User Choice	RBR/HBR: Setting 0 HBR2/3: User Choice
3-12 Total Jitter	RBR/HBR: All settings HBR2/3: User Choice	RBR/HBR: Setting 0 HBR2/3: User Choice
3-14 Main Link Frequency	Setting 2	Setting 0
3-15 SSC Modulation Frequency	Setting 2	Setting 0
3-16 SSC Deviation Accuracy	Setting 2	Setting 0

Take-away: lots of combinations for testing.

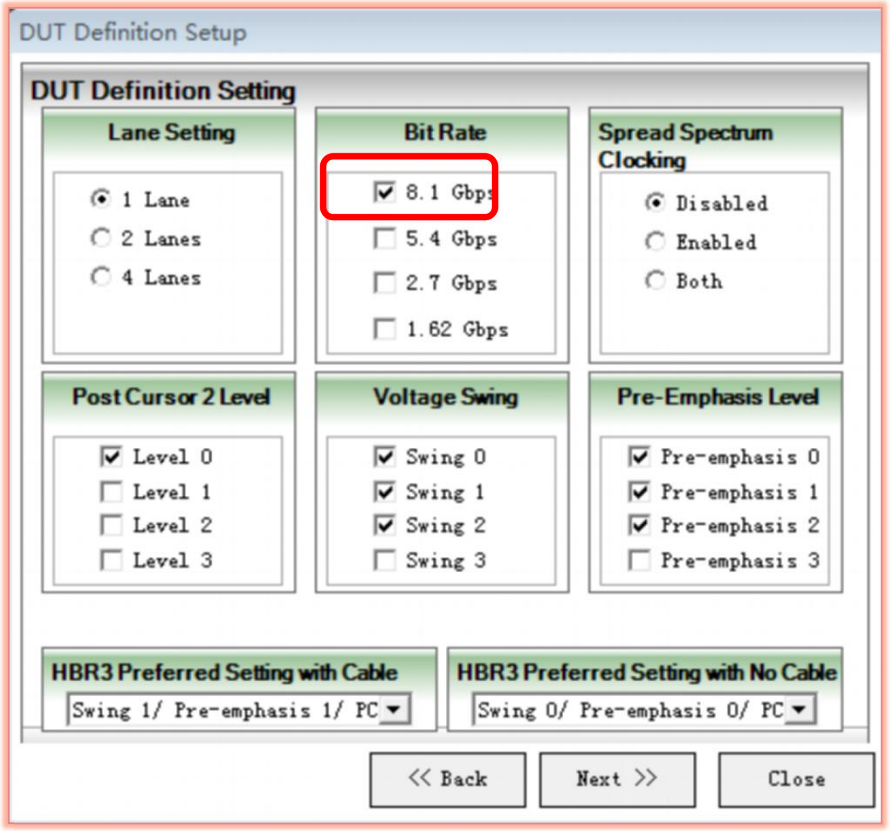
DisplayPort Source Tests Facilitation



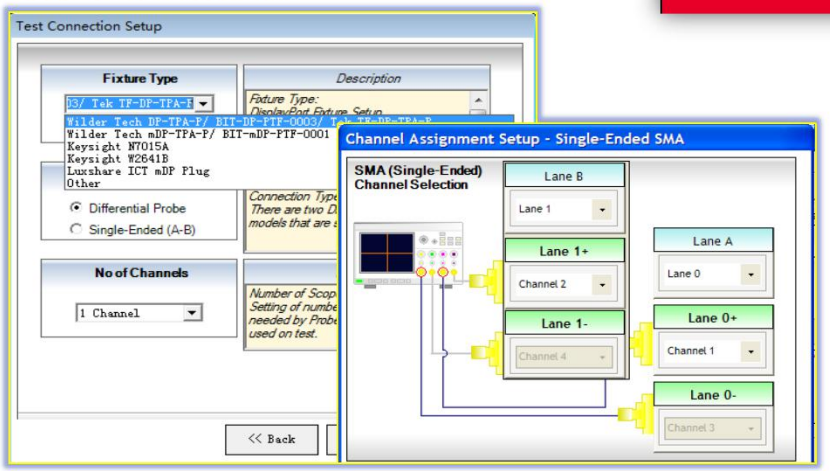
DisplayPort Source Tests Facilitation

- Device Definition to Run Test

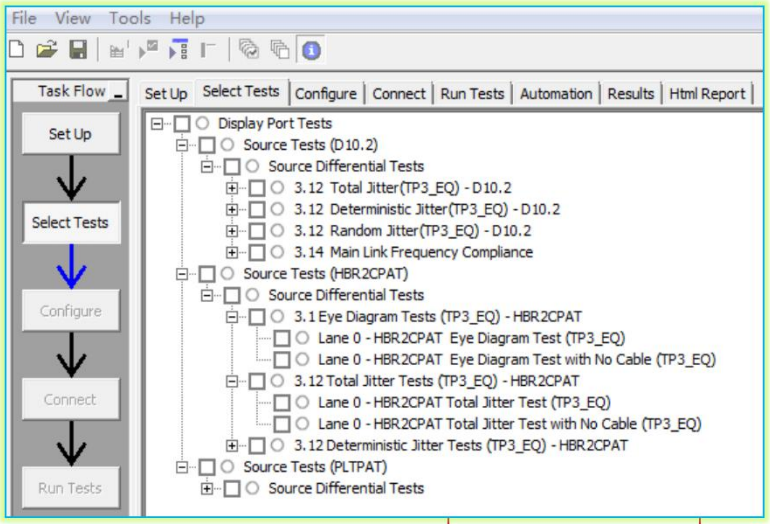
Device Definition



Test Connection



Test Selection



KEYSIGHT TECHNOLOGIES

Know that there are many test conditions!

- **Eye Diagram:**
- *One Level, One P-E setting, 2 SSC states, 4 Lanes, 4 bit rates, two cable conditions for HBR2/3: 2*4*4 +8+8 = 48 Eye Diagrams!*

DP1.4 incremental: 16 more tests

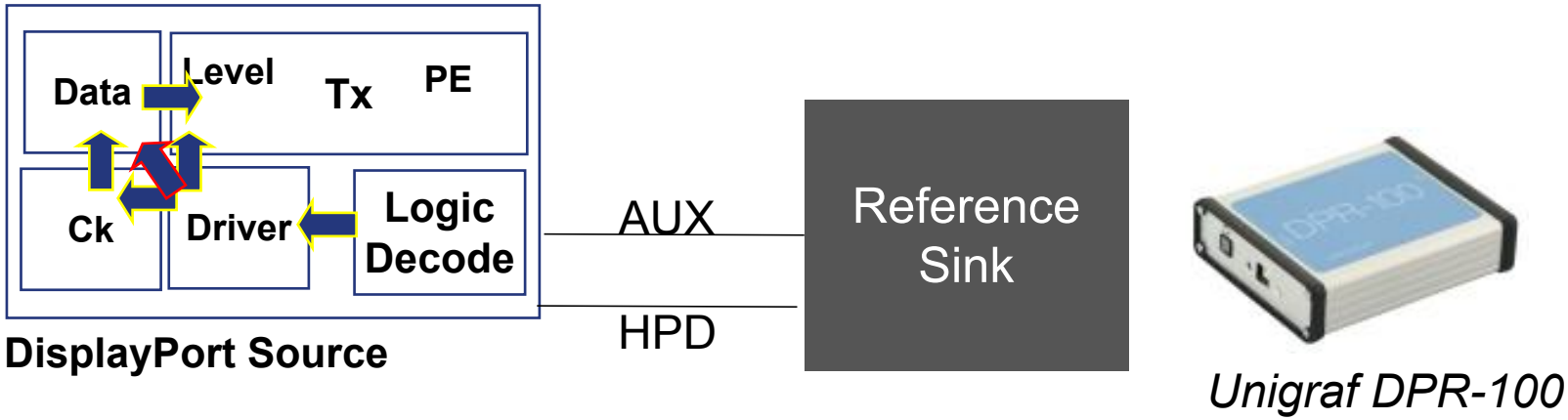
- **Pre-Emphasis Tests:**
- *10 combinations between Level and Pre-Emphasis, 4 bit rates, 2 SSC states, 4 lanes = 320 Tested states!*

DP1.4 incremental: 80 more tests

The details of test are handled by compliance test application test plan capability

Automation considerations

In order to test without manually setting the many conditions, a means to control bit rate, pre emphasis, and level is required. Need a device that acts like a sink but is very controllable. This is called a Reference Sink.



1. **DP1.4 testing requirements may NOT use TEST MODE but use an abbreviated link training process to control level, bit rate, and pre-emphasis.**

2. **The test application communicates with DPR100 to set DUT to correct state according to the test plan**

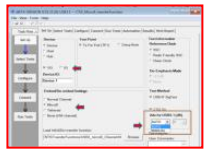
DisplayPort1.4 Source Testing

Considering the USB Type-C environment

C

N7015A

High Speed Lanes



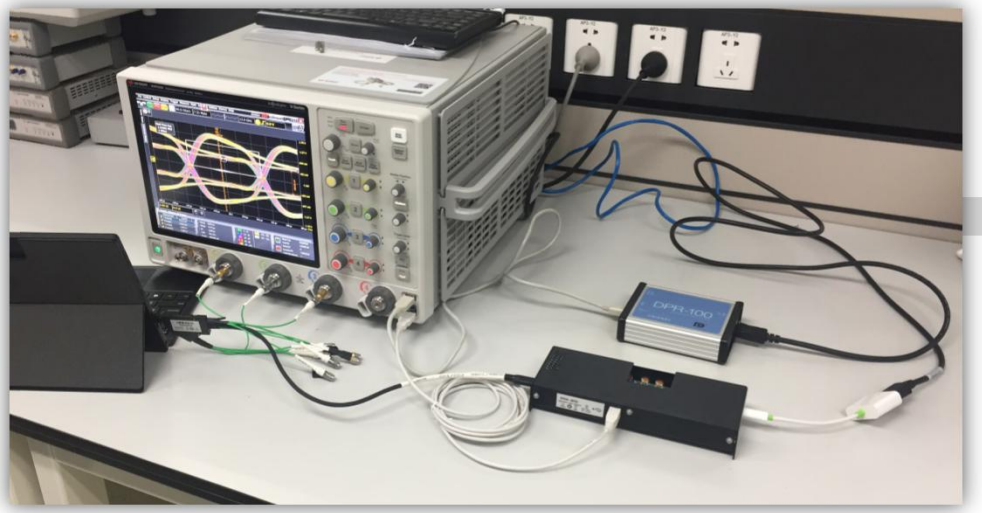
Infiniium Oscilloscope
BW=16GHz
Infiniisim
Equalization
Jitter
Clock Recovery
InfiniiScan
U7232D SW
Precision Probe

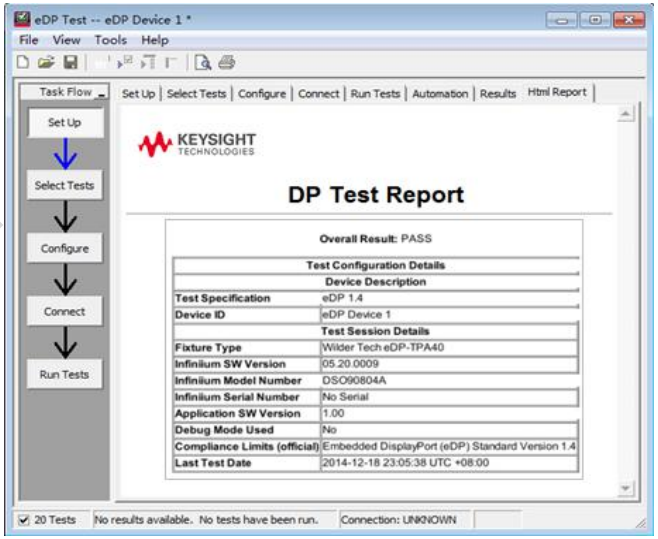
AUX Lane

N7016A

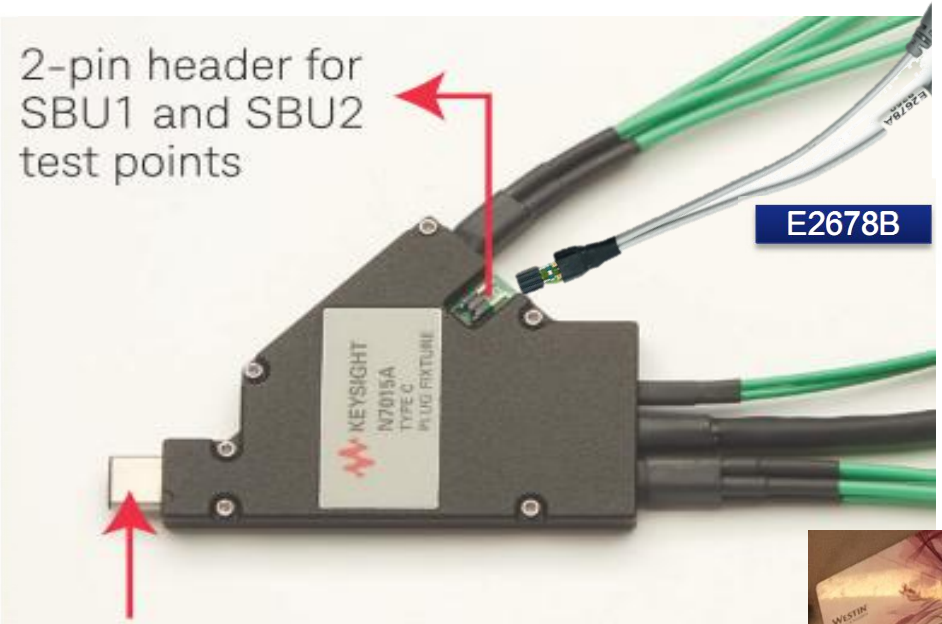
USB C to DP cable

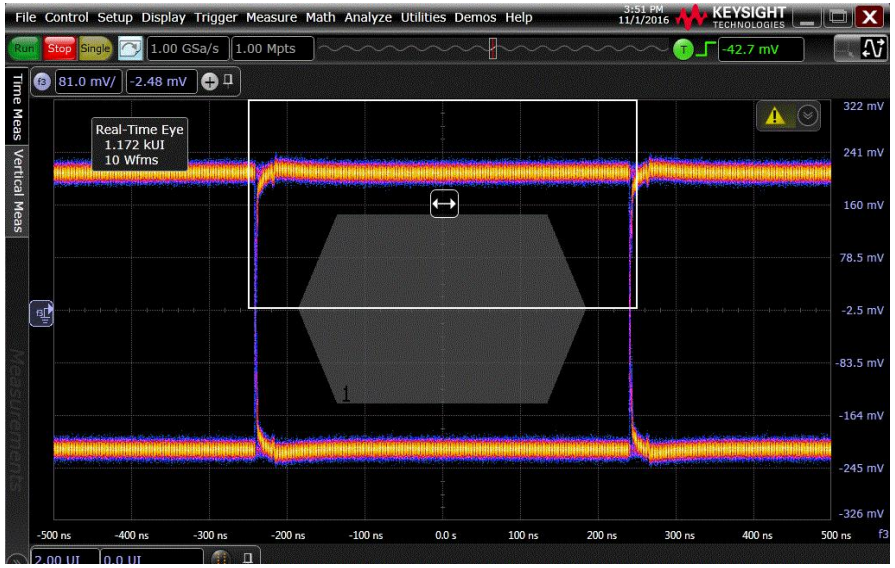
Unigraf DPR-100
Reference Sink

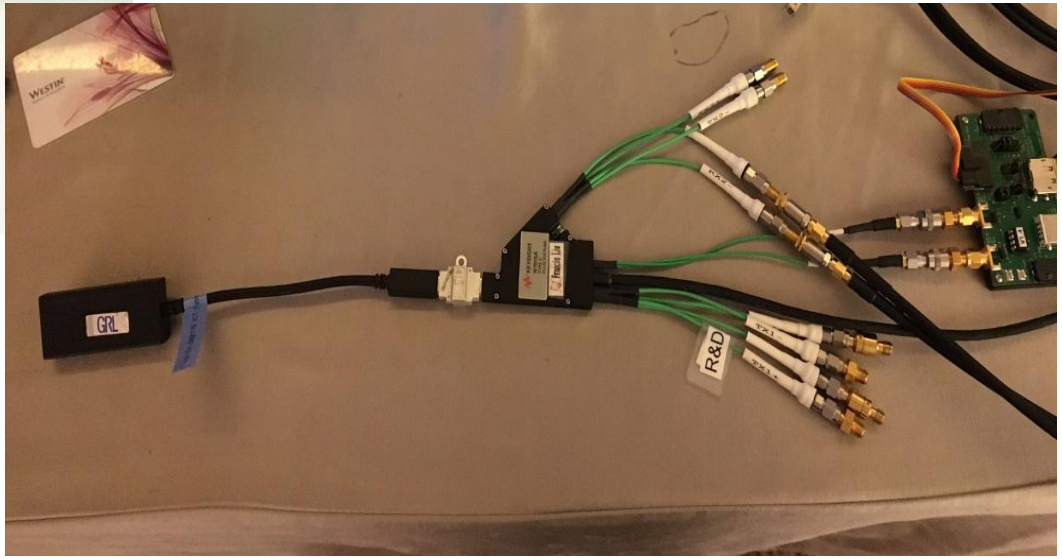




AUX Channel Testing







Take-away: AUX channel is very robust but its access and measurement has presented problems to our customers. Keysight drove the new 3 pin headers for testing. They work.

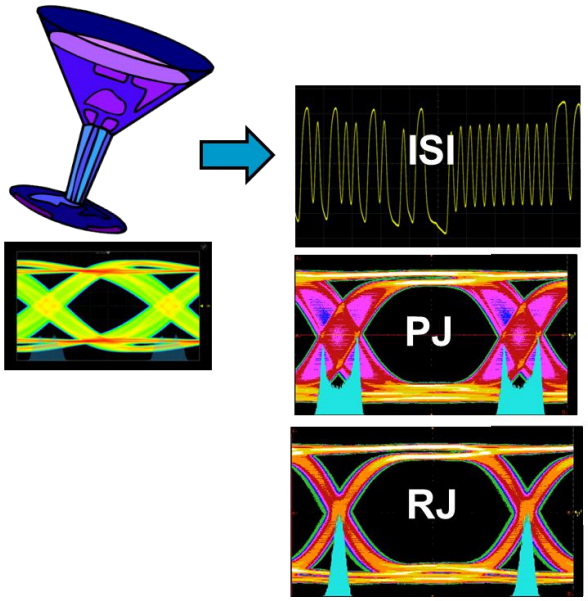
KEYSIGHT TECHNOLOGIES

DisplayPort Sink Testing

Sink Jitter Tolerance which provides a stressed signal of known pattern to the DUT and the DUT measures the number of bit errors. Sink Jitter Tolerance is performed ONE LANE at a time.

The Stressed Signal:

- A maximum Eye Height is specified
- A maximum Eye Width is specified

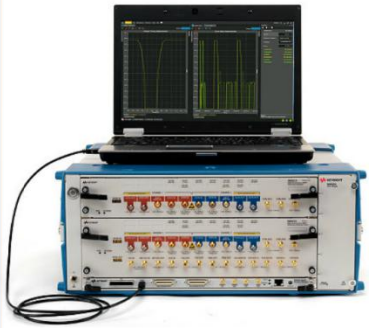


These conditions are achieved with a cocktail of jitter (RJ, SJ, ISI), Crosstalk or injected signal, and level control and the process is detailed in the Compliance Test Specification.

f(SJ)	TJ(JTHBR2rx)	ISI	RJ(RMS)	Approximate SJ_{SWEEP}	SJ_{FIXED} @ 200MHz
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]	[mUI]
2	1026	220	16.7	505	100
10	636	220	16.7	116	100
20	624	220	16.7	104	100
100	620	220	16.7	100	100

Table 4.4 from DisplayPort CTS 1.2b

DisplayPort Sink Testing



Pattern Generator

Reference Source

Lane Under Test

Main Link

AUX 1 Differential Lane

Hot Plug Detect

Bit Recovery

Data

DPCD

EDID

Interrupt

DisplayPort Sink

DisplayPort Sink

Expected Patterns

Bit Error

DPCD Reg

Bit Errors

Test Pattern

EQ

CDR

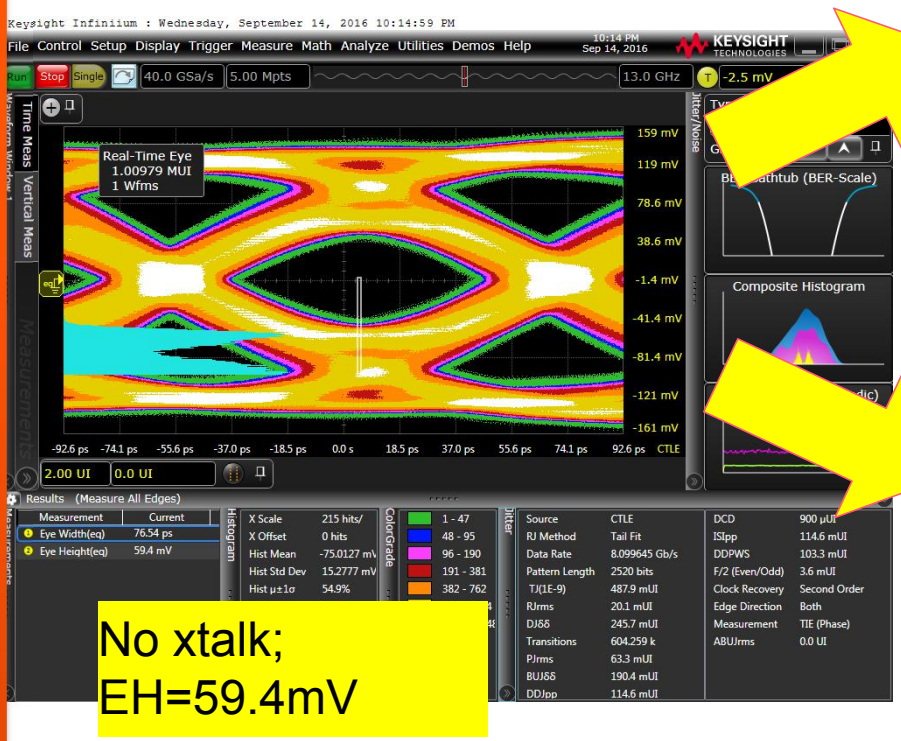
Freq Lock
Symbol Lock

Ck_{DR}

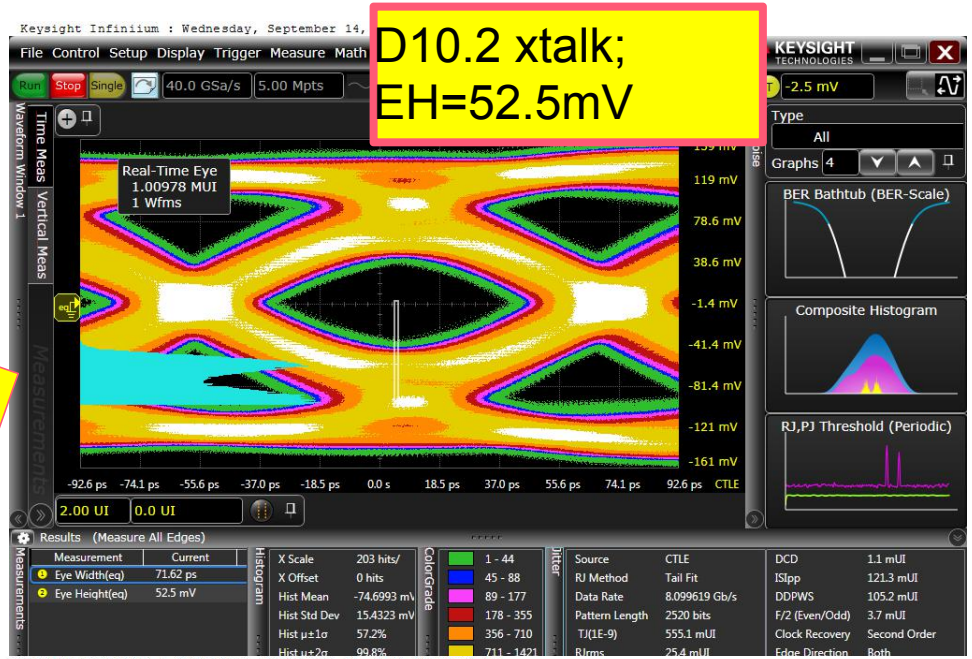
Display

Aggressor pattern comparison

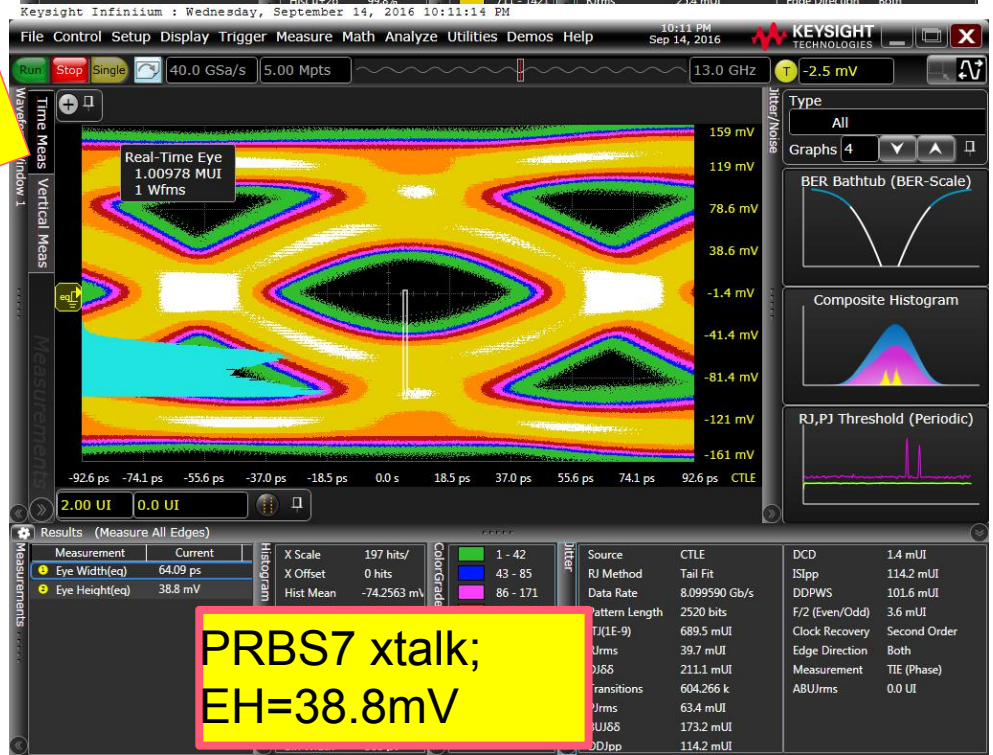
Clock vs PRBS7



No xtalk;
EH=59.4mV



D10.2 xtalk;
EH=52.5mV



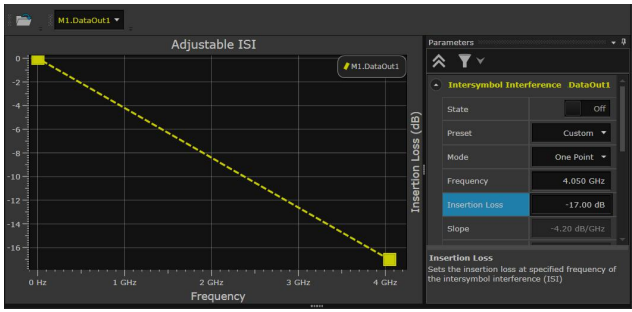
PRBS7 xtalk;
EH=38.8mV

KEYSIGHT TECHNOLOGIES

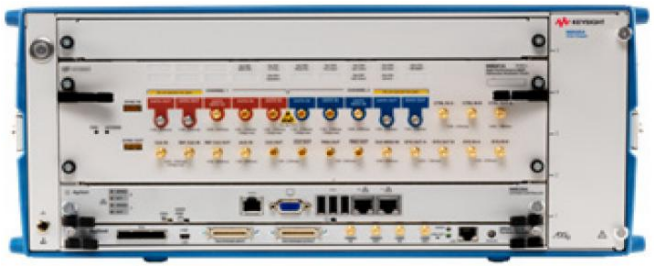
Unique features in the market

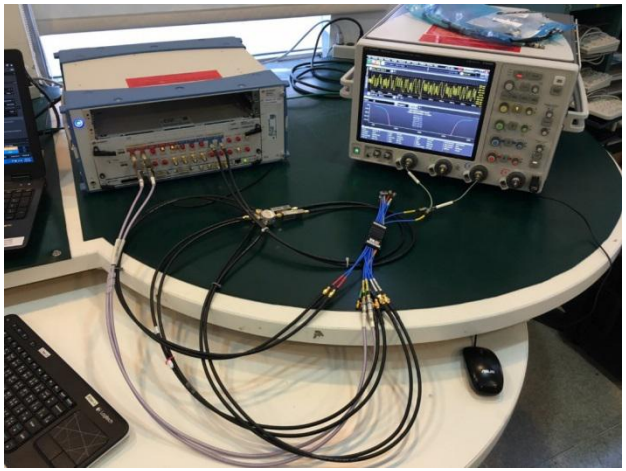
Why M8020A is better in DP sink testing

– Keysight provide the adjustable ISI capability to accurate meet the ISI jitter target requirement, the HW (PCB trace, cables) adjustment for target ISI jitter is very painful and cable, connector physical character will change with time.



– Only M8020A can provide the 2nd output channel to fit the crosstalk aggressor requirement, which are Non-Sync with victim rate and TPS4 pattern at 8.1 Gbps (See next slide)





KEYSIGHT TECHNOLOGIES

Type-C DisplayPort Technologies

- ✓ Test Validation will have to consider new forces present in our industry
  - ✓DP1.4 is increasing the data rate and modifying the Reference equalizer.
  - ✓The Industry is moving to USB Type C. The DP over Type C, 'DP Alt mode specification', targets this connector and may be the dominant use model.
- ✓ Complexity for validators abounds.
  1. Type C: multiple protocols to be tested.
  2. Power now a consideration: provider, consumer, arbitrary voltage, current
  3. Orientation changeable: test coverage requirement will increase.
  4. Switching networks for unattended test: calibration, maintenance.
- ✓ We are waiting for the CTS coming. Aggressive test time reduction, will change test plans.
- ✓ While the type C connector will delight consumers, validation will require extensive characterization and compliance regimen. Start Early!

Agenda

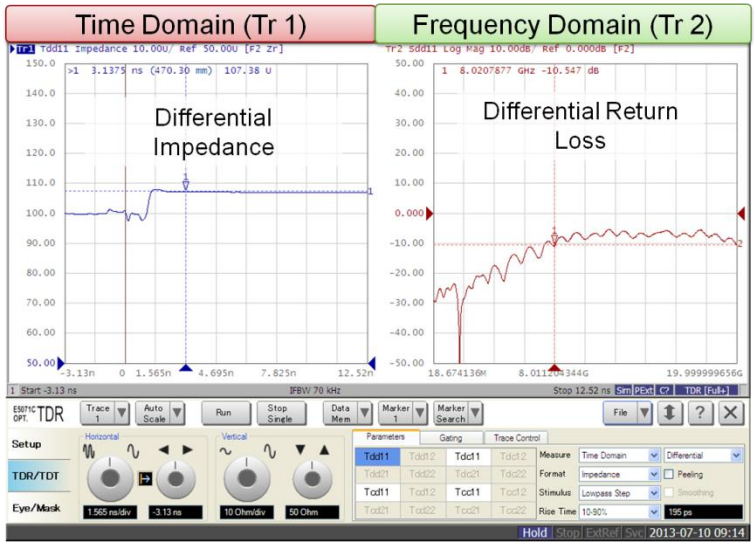
- Type-C 简介
- HDMI1.4b over Type-C
- DP over Type-C
- 阻抗和Type-C电缆测试介绍
- Final Words

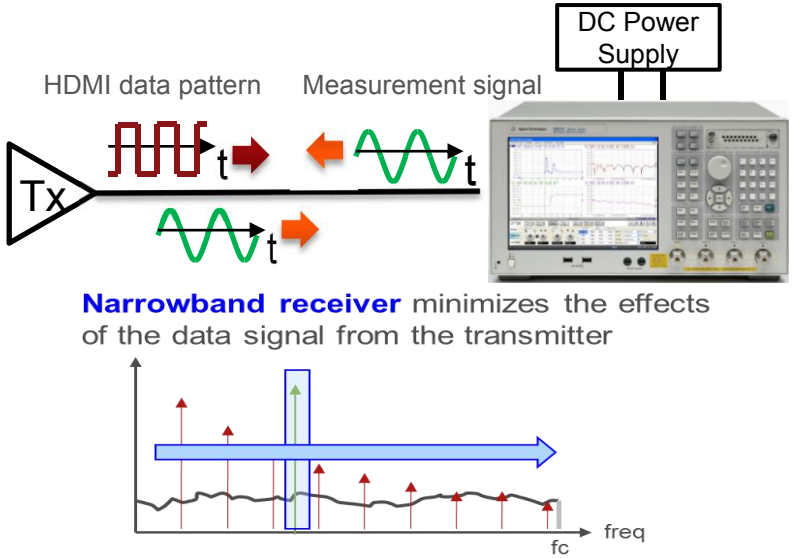
Physical Layer *Source/Sink Impedance* Testing

Points to Know:

New

- Impedance measurements of Source and Sink required in HDMI2.0
- Source *impedance measurements during transmission of actual data pattern (Hot TDR measurements)* is required
- DC voltage bias can be applied through internal bias-tees
- Hot TDR with ENA-TDR, fast, accurate and no worry about ESD

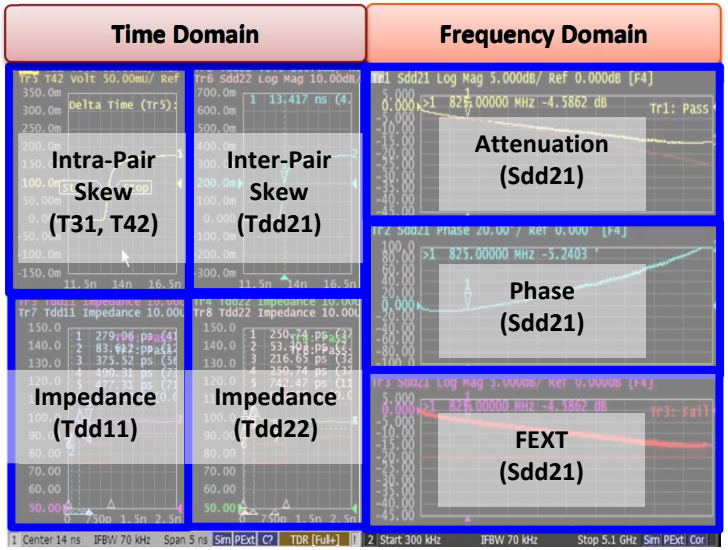


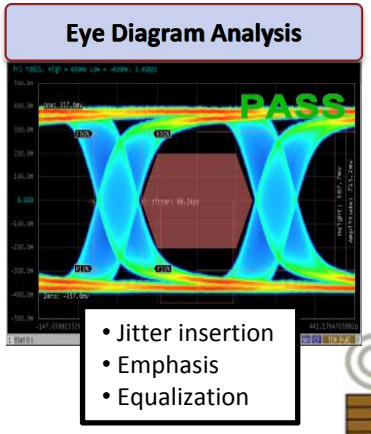


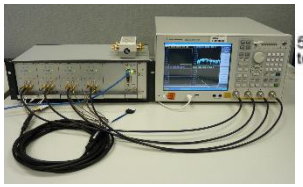
Physical Layer Cable Assembly Testing

Points to Know:

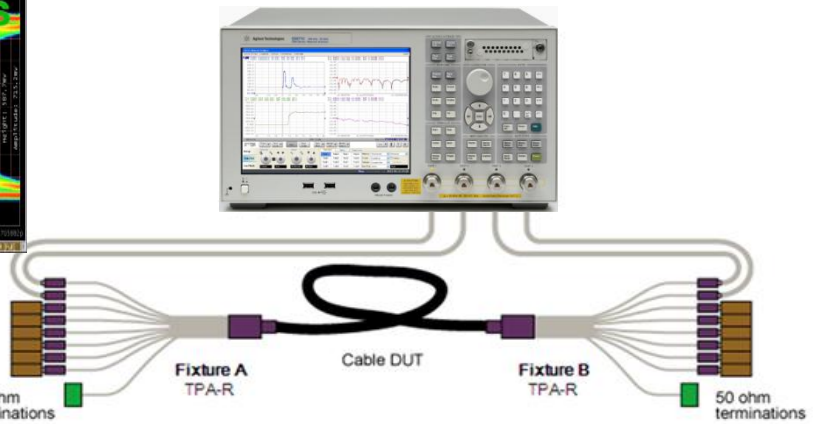
- HDMI2.0 doesn't require new cable testing; still follows HDMI1.4b spec
- Standard Cable measurements for characterization and compliance testing: skew, impedance, attenuation, and crosstalk.
- "Stressed" Eye Diagram Analysis of Interconnects: allowing direct measurement of eye characteristics at the end of the link.
- *Optional switch and test automation software available from Solutions Partner BitifEye*



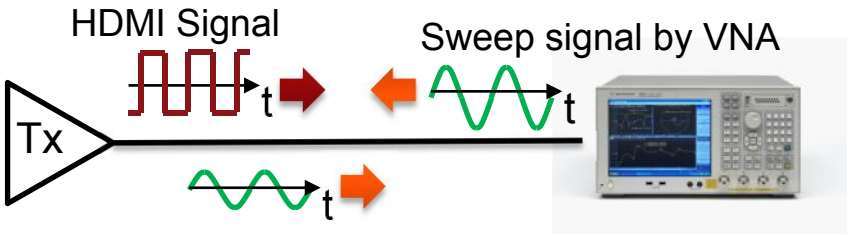




Complete characterization of interconnects
(Time domain, frequency domain, and Eye diagram)

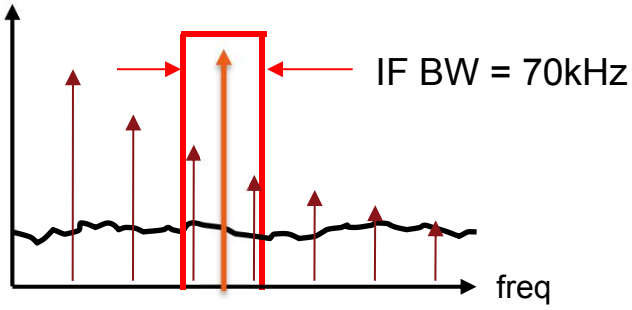


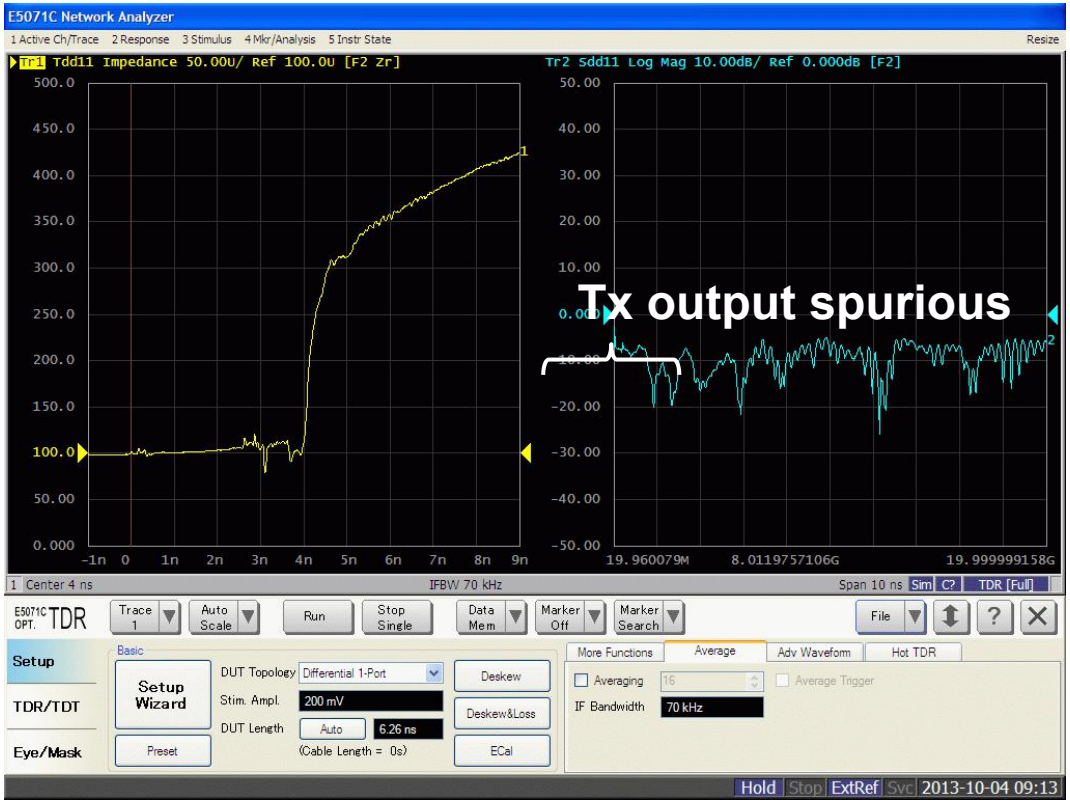
Hot TDR Issue: Bad effect of Tx output signal



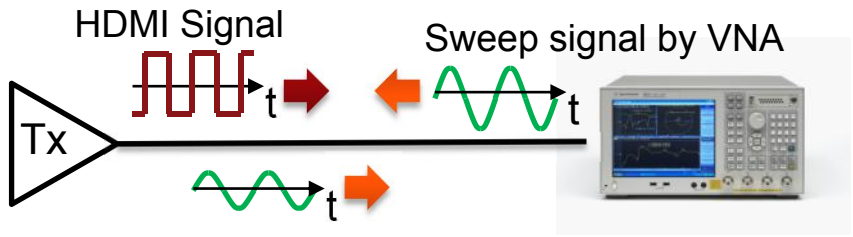
TDR impedance test result varies due to output signal from Tx

Tx output signal is also input to the VNA's receiver and affects test result.

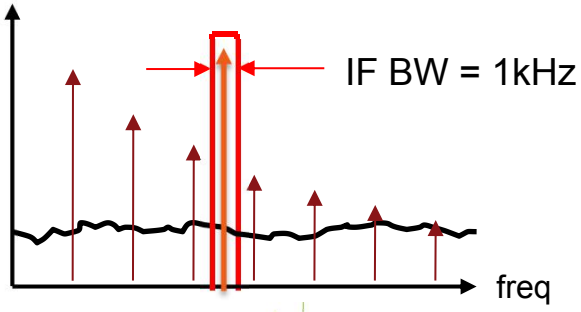


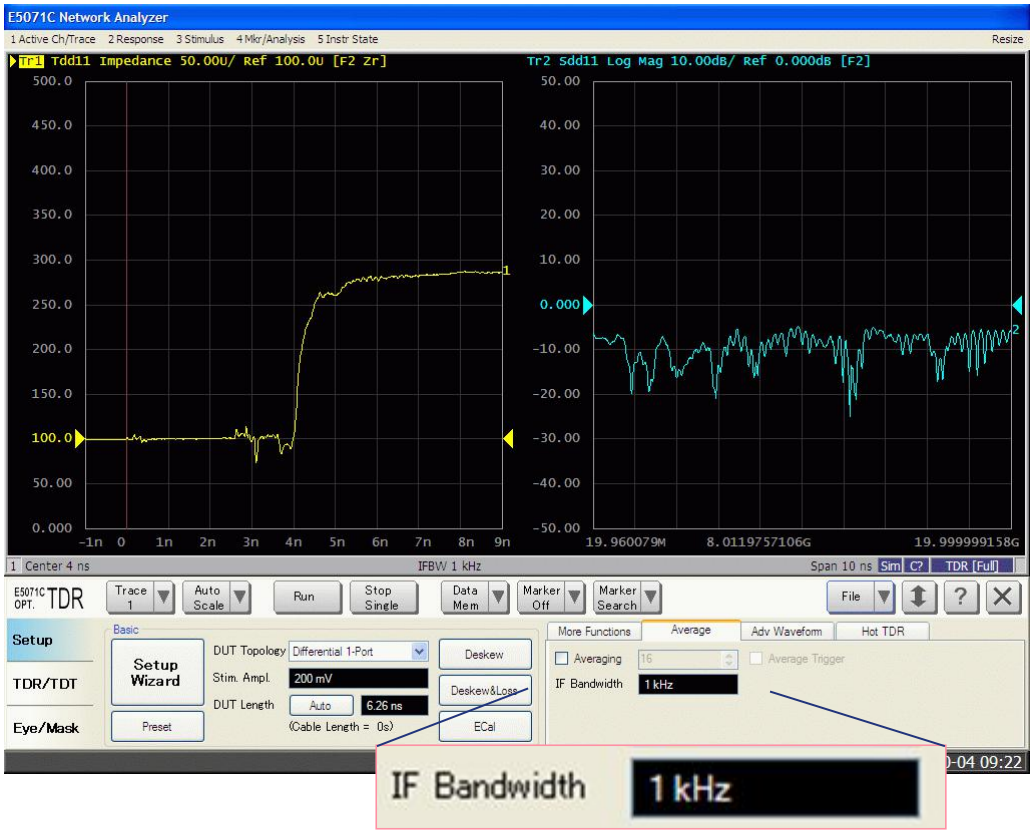


Hot TDR Issue: Bad effect of Tx output signal



Tx output effect can be minimized by narrowing IF BW (receiver filter bandwidth)





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- HDMI1.4b over Type-C
- DP over Type-C
- 阻抗和Type-C电缆测试介绍
- Final Words

Keysight 数字总线标准专家组

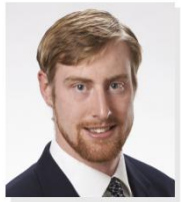
Keysight experts helping define next generation standards, and solutions

Memory Perry Keller	DisplayPort Brian Fetz	USB Jit Lim	Computer Rick Eads	Optical Greg LeCheminant	HDMI Stefan Friebe	Storage Matthew Woerner	MIPI Roland Scherzinger
Board of Directors JEDEC **Compliance Chair** UFSA	**Board of Directors** VESA **Contributor** VESA Phy Sub Group	**Contributor** USB-IF Thunderbolt	**Board of Directors** PCI-SIG	**Contributor** IEEE, OIF-CEI, T11 FC	**Contributor** HDMI	**Contributor** SATA-IO, T10 SAS	**TSG Member** **UniPro Vice Chair** MIPI Alliance
LPDDR4, UFS	**DP 1.4 Type-C**	**USB 3.1, Thunderbolt 3**	**PCIe G3, G4**	**PAM-4, CEI 3.1**	**HDMI 2.0**	**SATA, SAS-3**	**D/M/C–PHY, UniPro**



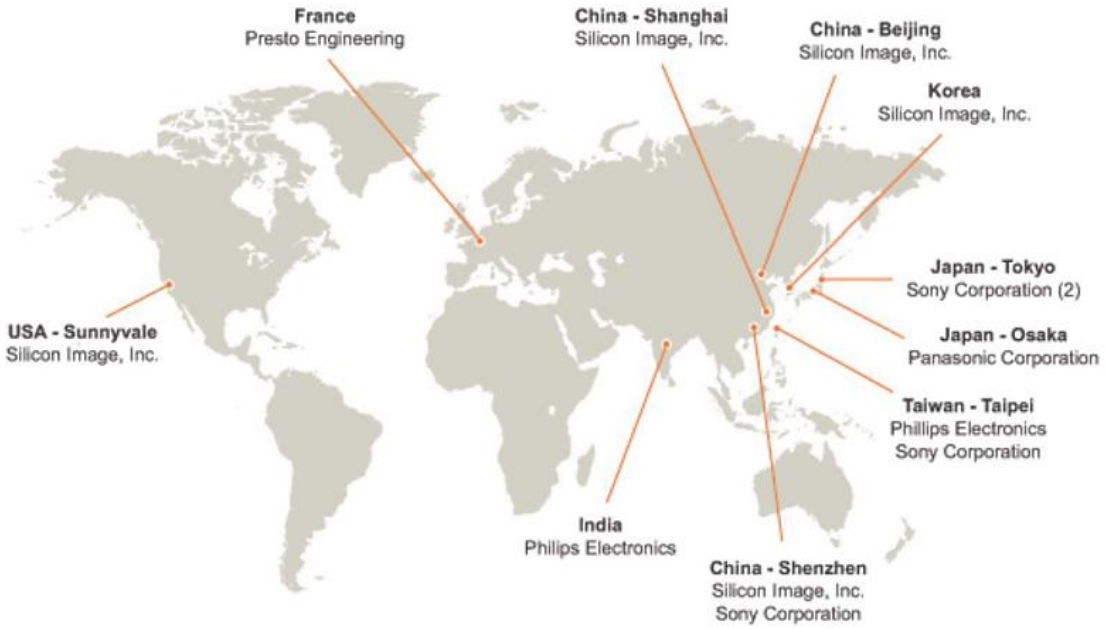


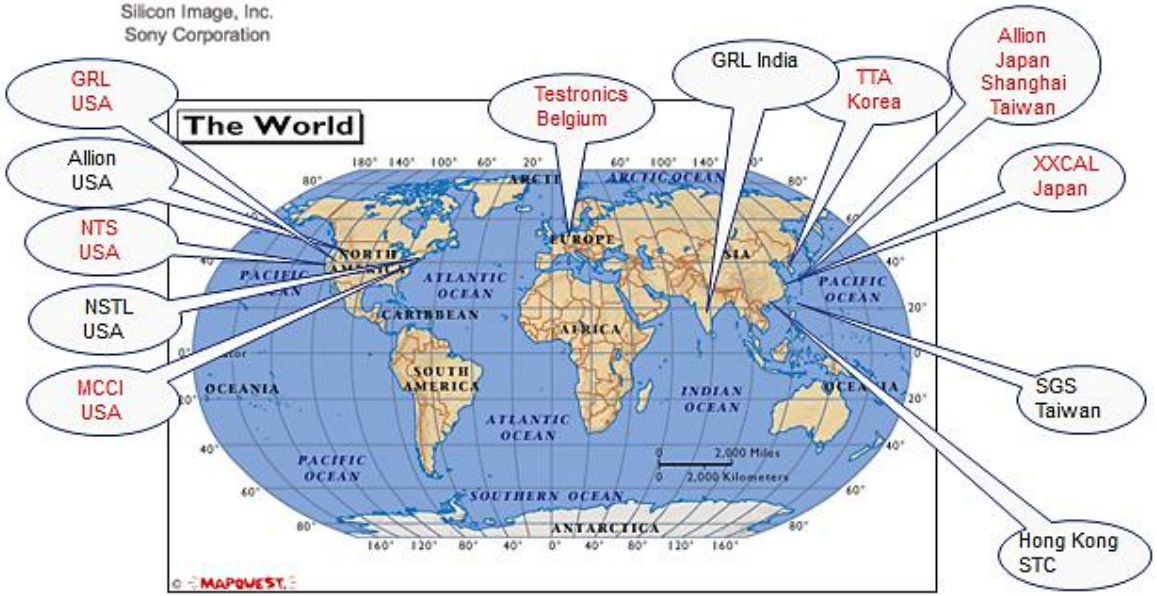





Keysight 对全球认证测试实验室的支持

Authorized Test Centers

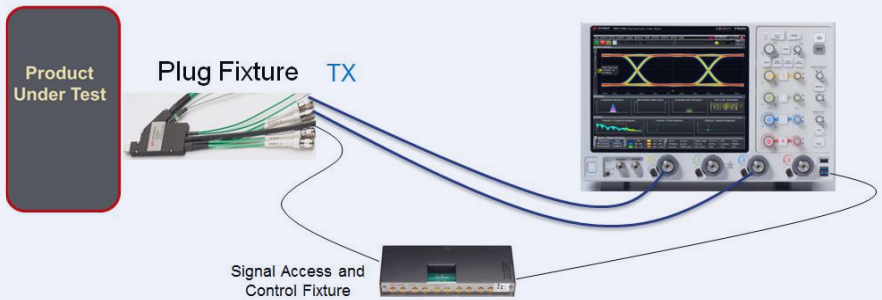




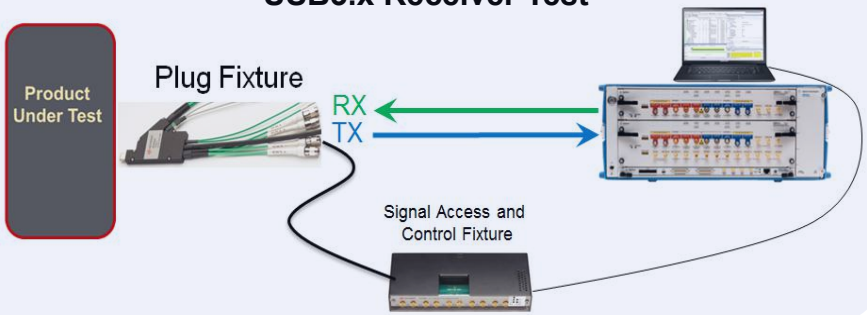
KEYSIGHT TECHNOLOGIES

Type-C™ USB, DisplayPort, PD 解決方案

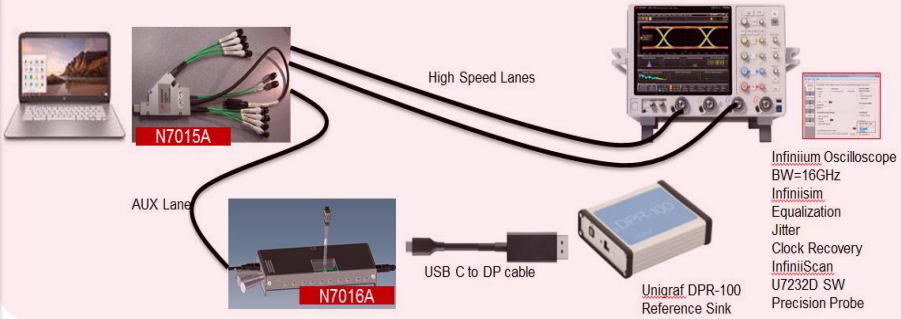
USB3.x Transmitter Test



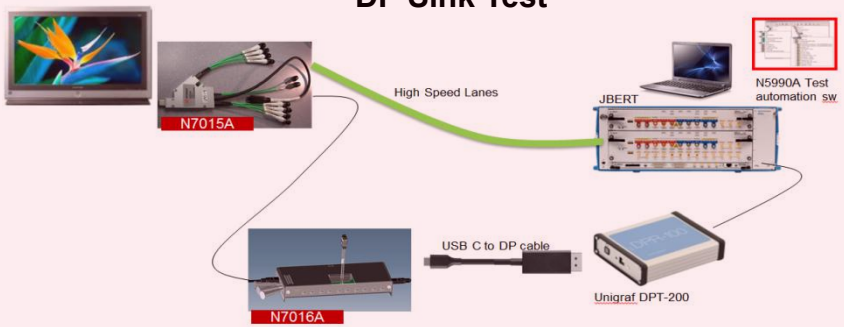
USB3.x Receiver Test



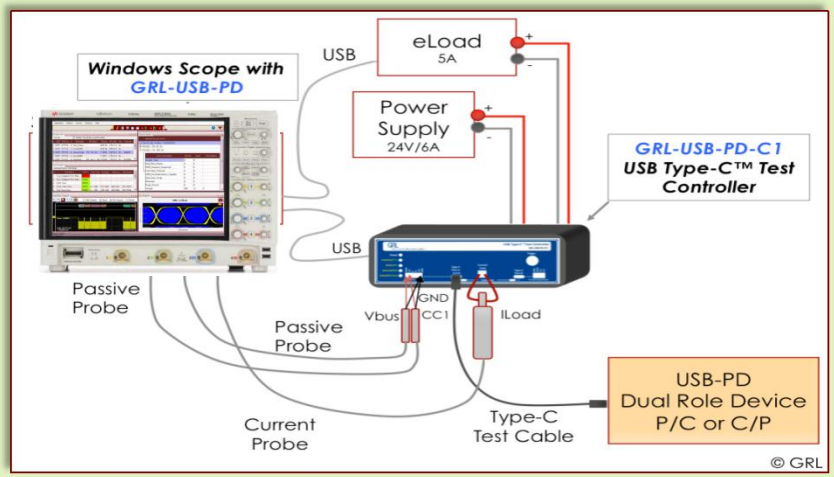
DP Source Test



DP Sink Test



Power Delivery Test



KEYSIGHT TECHNOLOGIES

Keysight Type-C Solution Advantage

中国的数字测试认证测试中心全面采用是德科技测试方案

HDMI国内共四家认证测试中心，两家预认证测试中心，100%用Keysight测试方案

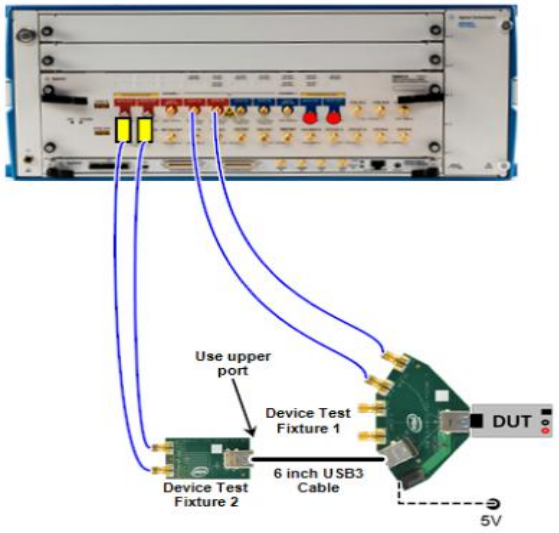
- Simplay Lab Shanghai 认证测试中心 (HDMI , MHL)
- Simplay Lab Shenzhen 认证测试中心(HDMI , MHL)
- 深圳数字电视国家工程实验室 (GRL授权)
- CESI Beijing 认证测试中心(HDMI , DP , USB)
- MediaTek Shanghai 预认证测试中心
- Sunplus Shenzhen 预认证测试中心

USB 国内共三家认证测试中心，都采用了Keysight测试方案

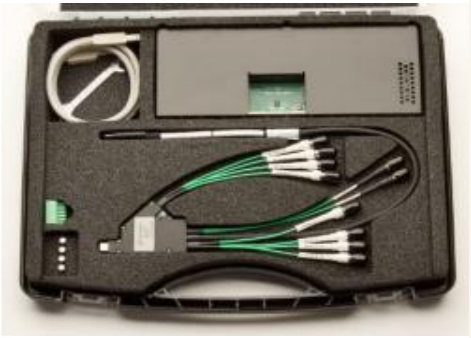
- HKSTC 认证测试中心 ，仅用Keysight测试方案
- SGS认证测试中心 ，仅用Keysight测试方案
- CESI Beijing 认证测试中心, 仅用Keysight测试方案
- ALLION 拥有包括Keysight在内两个公司的测试方案，但其美国分公司100%采用Keysight的方案，ALLION台湾Type C（USB3.1/DP/TBT）测试使用且仅用Keysight方案

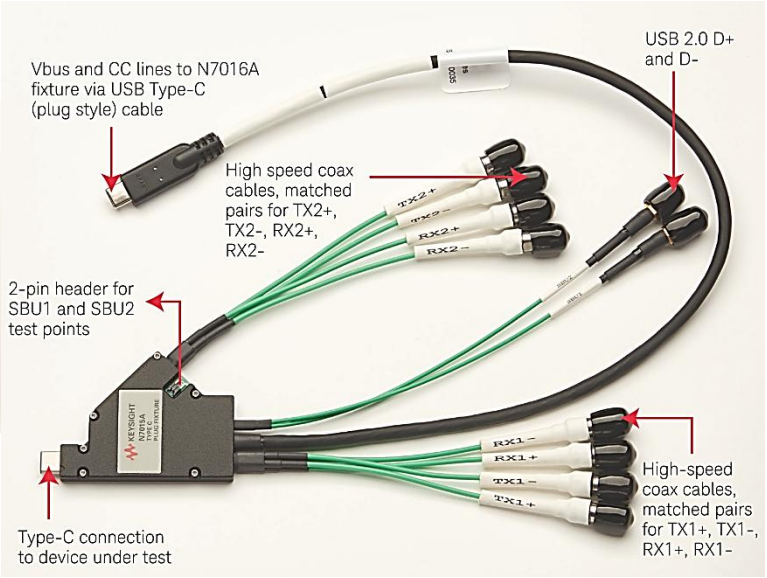
shenzhen. HDMI-ATC.COM　STC 标檢　SimplayHD　HDMI 上海 授权测试中心 SHANGHAI HDMI AUTHORIZED TEST CENTER

Keysight Receiver Test Solution



Keysight Type-C Fixture





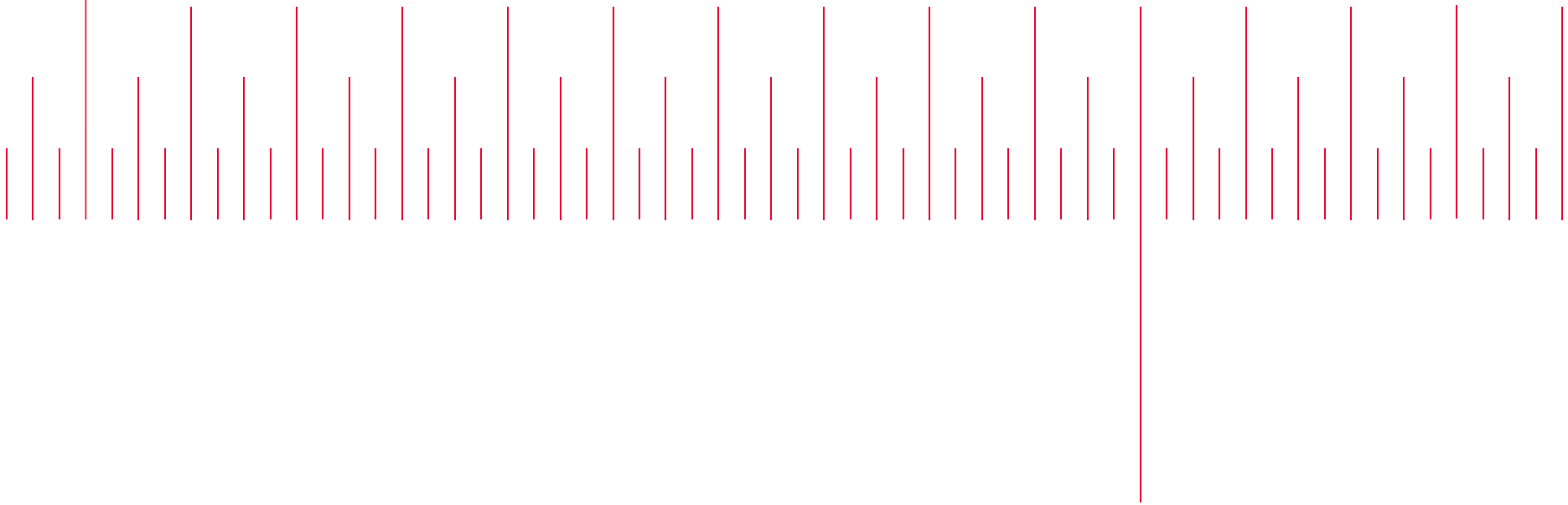
- *夹具兼容 USB3.1, DP1.4, HDMI2.0 TBT3, MHL等测试*
- *业内最好的信号完整性 : 20 GHz@-3dB*
- *提供 Tx 和 USB-PD测试用的测试点和探头连接处*

KEYSIGHT TECHNOLOGIES

Type-C™ Technology Key Messages

- USB Type-C **is not** USB 3.1
  - USB Type-C电缆和连接器规范是对USB 3.1规范的一个补充，无论如何，USB Type-C不是USB 3.1。这些术语不可以互换。
- USB Type-C **is not** USB Power Delivery
  - USB Power Delivery是一个协议/硬件的解决方案，可提升USB的供电能力高达100 Watt。这些术语不可以互换。
- 对于一个USB Type-C产品来说，它不是必须要支持USB Power Delivery和/或USB 3.1技术
  - USB Type-C设备制造商可以选择去支持USB Power Delivery 和/或USB 3.1能力，但不是必须的。

Thank You!



KEYSIGHT TECHNOLOGIES