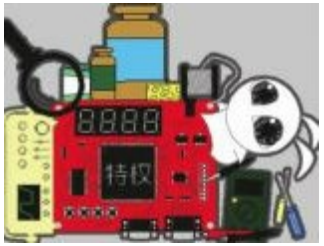


时序设计专题之二

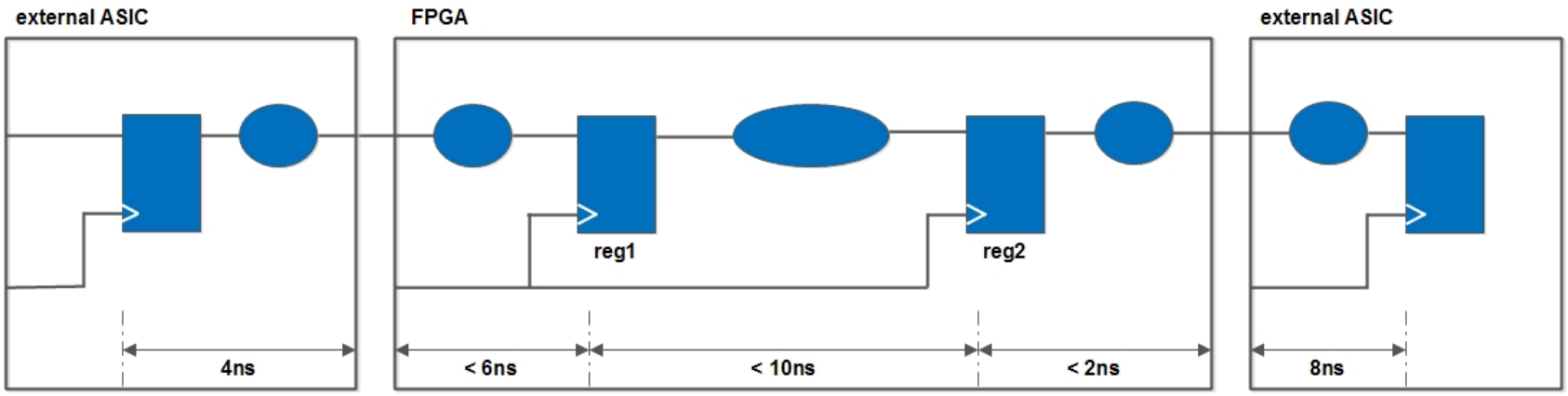
——PIN2REG时序分析

BY 特权同学

时序分析基础

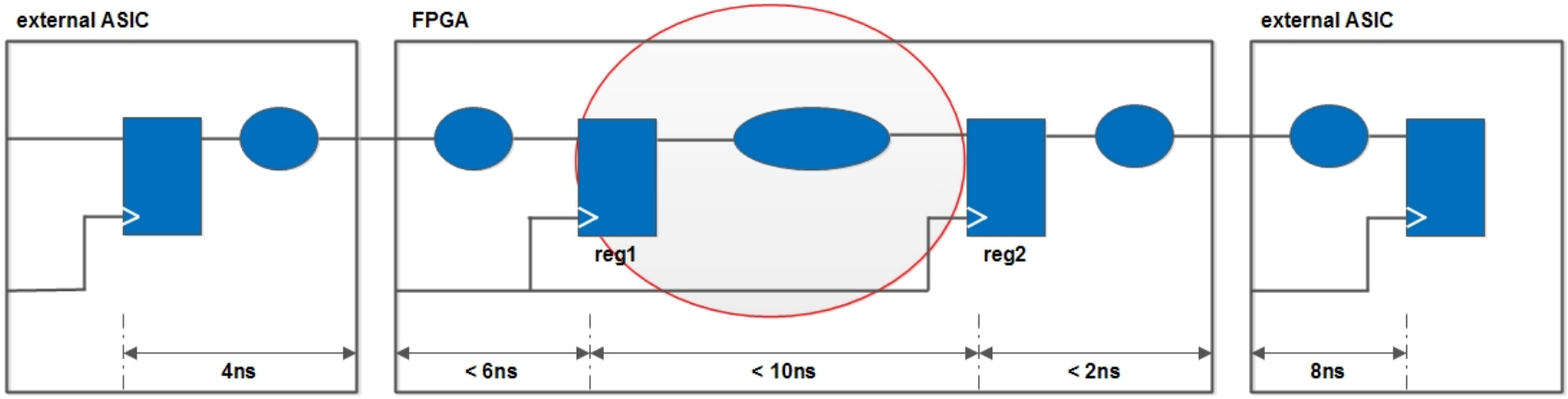
基本时序路径 —— 三类基本约束路径

- 输入信号 pin2reg
- 内部信号 reg2reg
- 输出信号 reg2pin



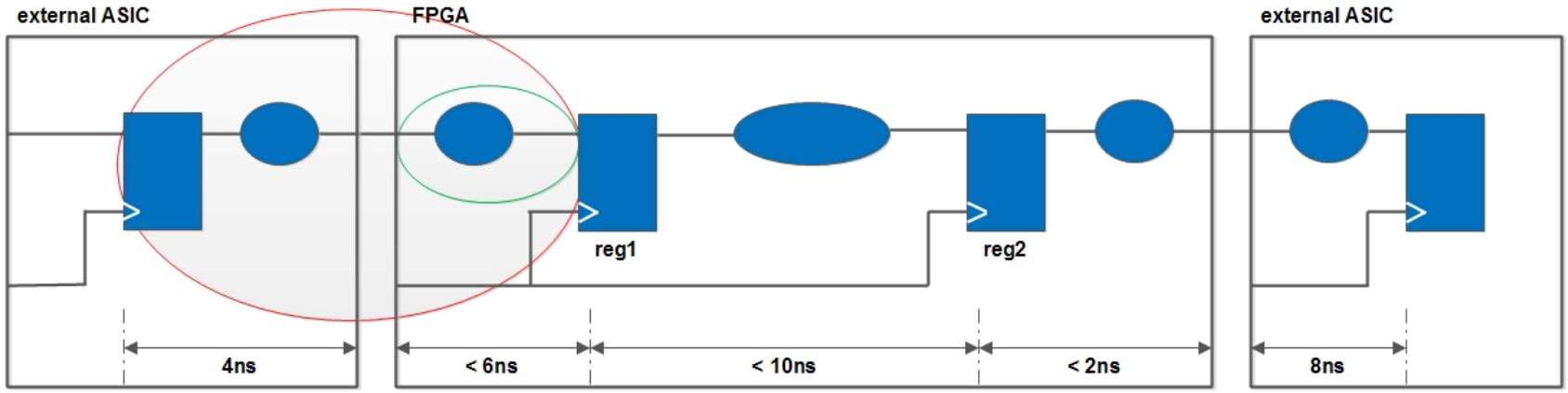
时序分析基础

基本时序路径 —— 寄存器到寄存器的路径（reg2reg）



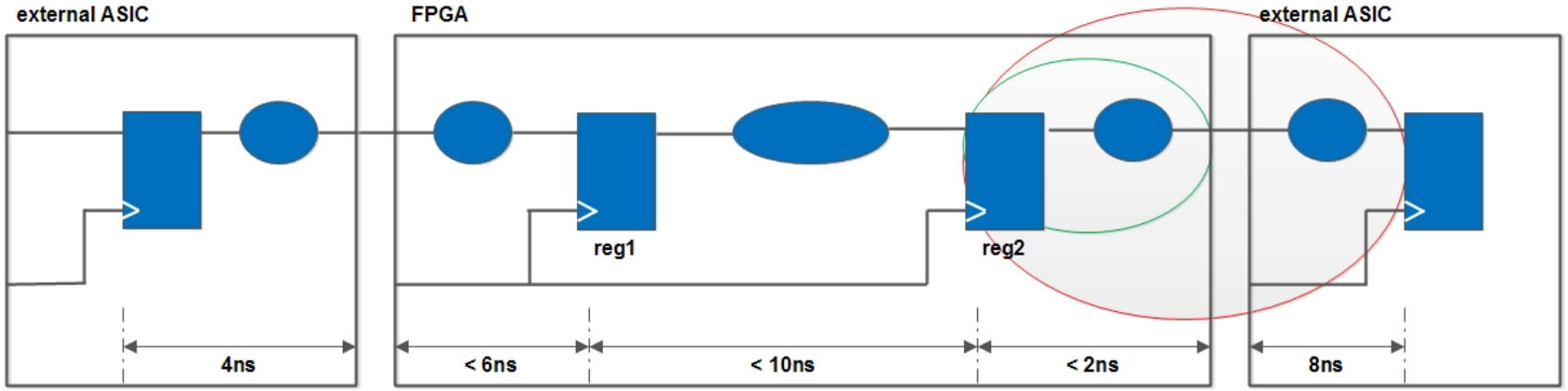
时序分析基础

基本时序路径 —— 管脚到寄存器的路径（pin2reg）



时序分析基础

基本时序路径 —— 寄存器到管脚的路径（reg2pin）

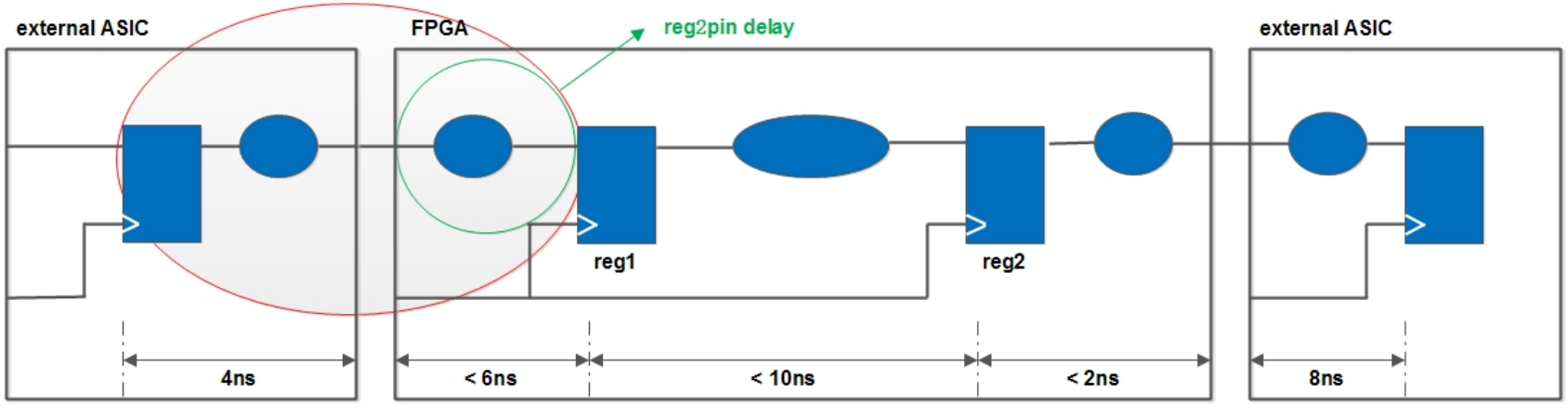


时序分析基础

基本时序路径 —— 管脚到寄存器的路径（pin2reg）

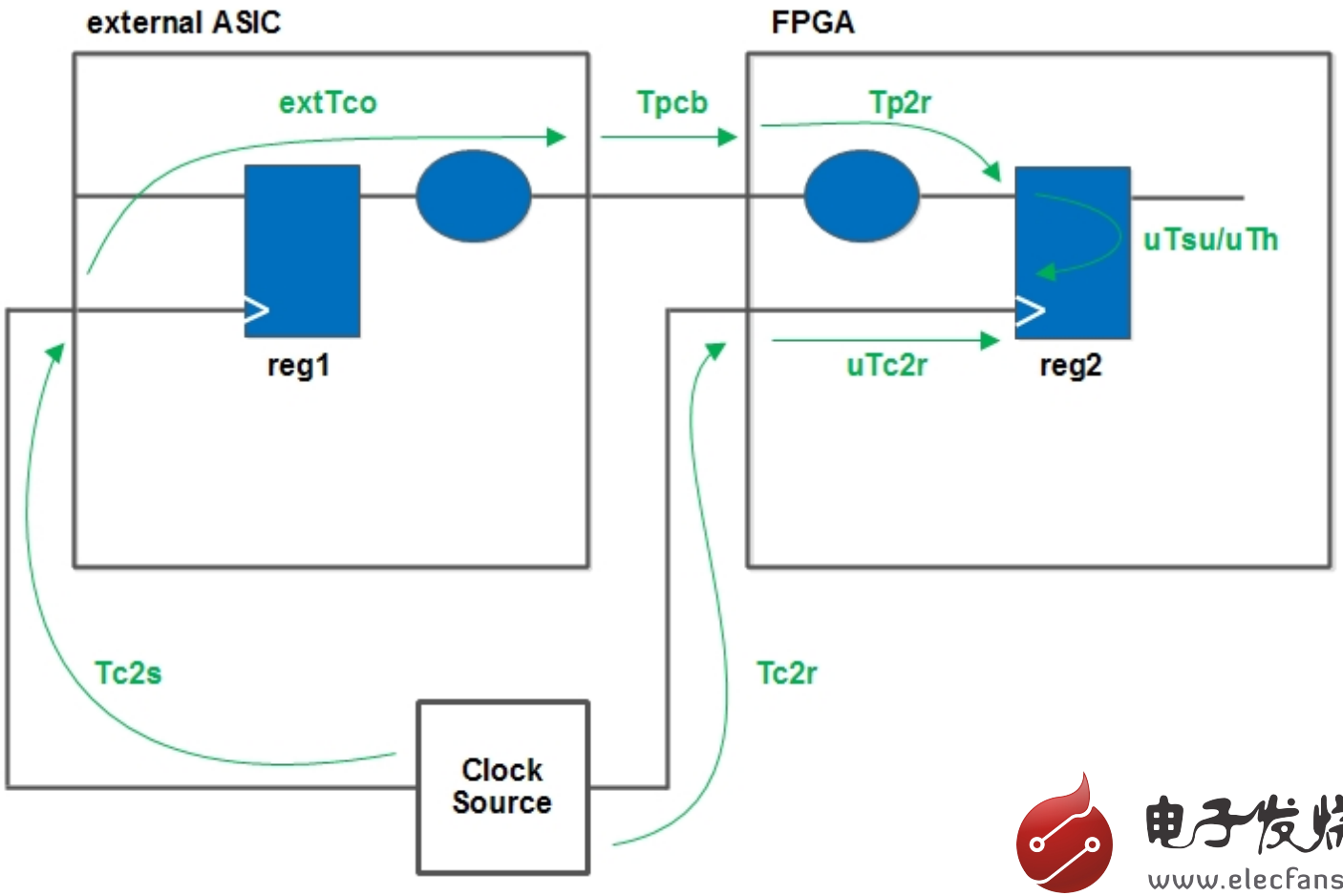
pin2reg约束值：

1. 直接约束取值4ns
2. 间接约束取值6ns



时序分析基础

基本时序路径 —— 管脚到寄存器的路径（pin2reg）



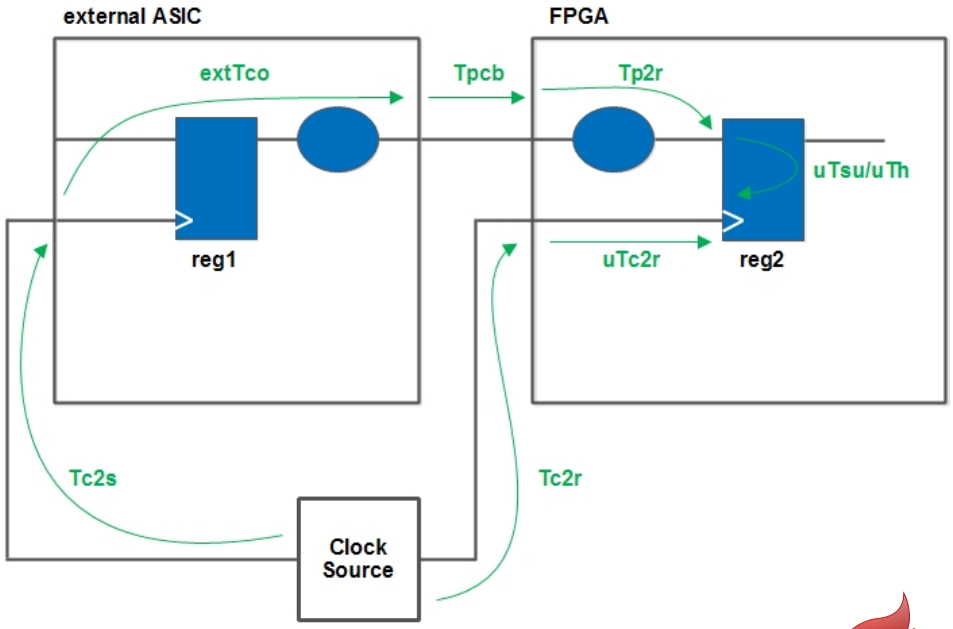
时序分析基础

基本时序路径 —— 管脚到寄存器的路径（pin2reg）

建立时间

Launch edge + Tc2s + extTco + Tpcb + Tp2r

< latch edge + (Tc2r + uTc2r) - uTsu



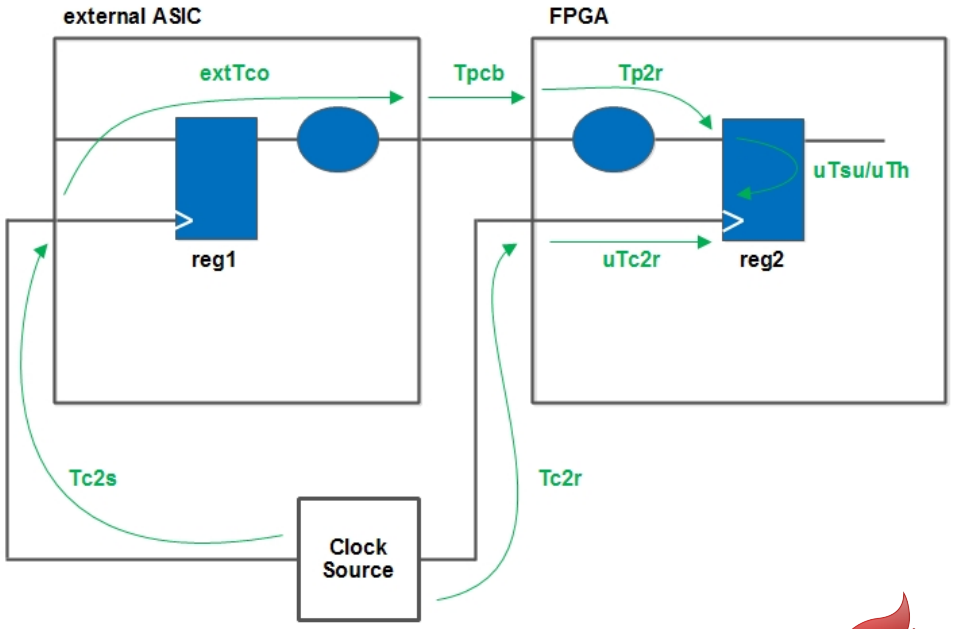
时序分析基础

基本时序路径 —— 管脚到寄存器的路径（pin2reg）

建立时间

(Tc2s - Tc2r) + extTco + Tpcb

< (latch edge - Launch edge) - uTsu + uTc2r - Tp2r



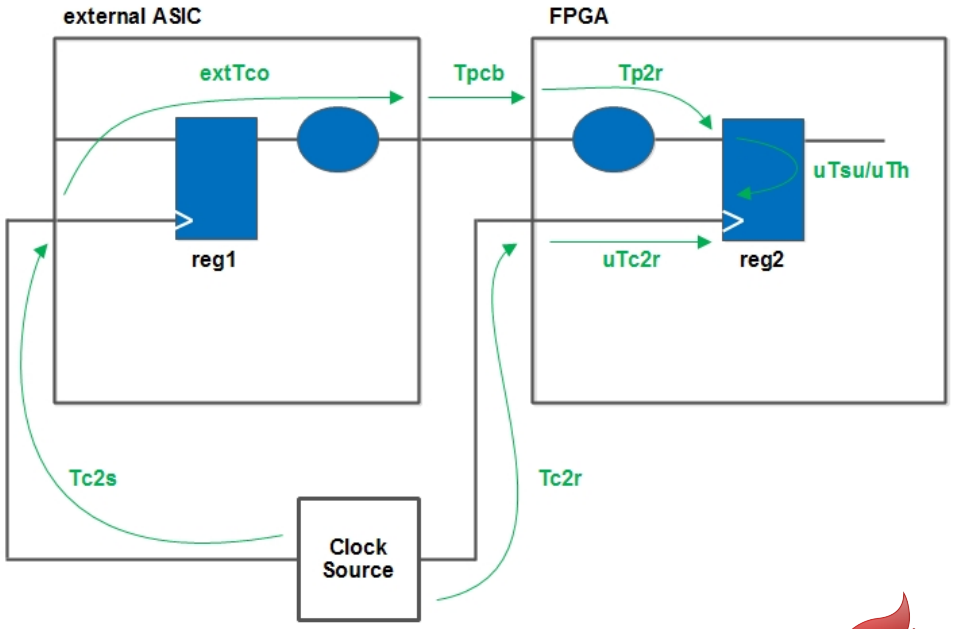
时序分析基础

基本时序路径 —— 管脚到寄存器的路径（pin2reg）

保持时间

Launch edge + Tc2s + extTco + Tpcb + Tp2r

> latch edge + (Tc2r + uTc2r) + uTh



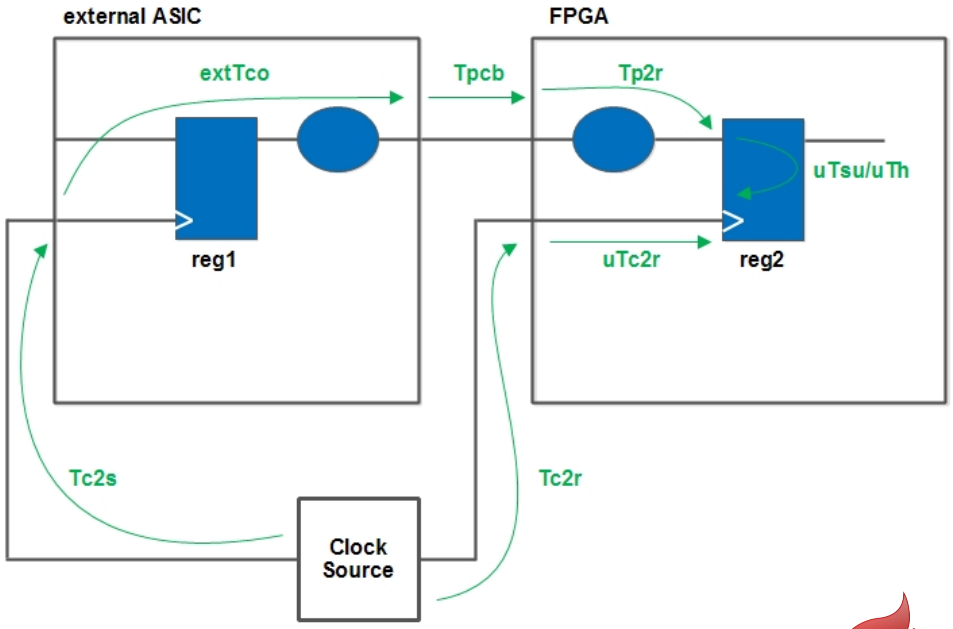
时序分析基础

基本时序路径 —— 管脚到寄存器的路径（pin2reg）

保持时间

(Tc2s - Tc2r) + extTco + Tpcb

> (latch edge - Launch edge) + uTh + uTc2r - Tp2r



时序分析基础

基本时序路径 —— 管脚到寄存器的路径（pin2reg）

(Tc2s - Tc2r) + extTco + Tpcb
< (latch edge - Launch edge) + uTc2r – uTsu - Tp2r
(Tc2s - Tc2r) + extTco + Tpcb
> (latch edge - Launch edge) + uTc2r + uTh - Tp2r

取input delay =
(Tc2s - Tc2r) + extTco + Tpcb
则input delay <
(latch edge - Launch edge) + uTc2r – uTsu - Tp2r
且input delay >
(latch edge - Launch edge) + uTc2r + uTh - Tp2r

时序分析基础

基本时序路径 —— 管脚到寄存器的路径（pin2reg）

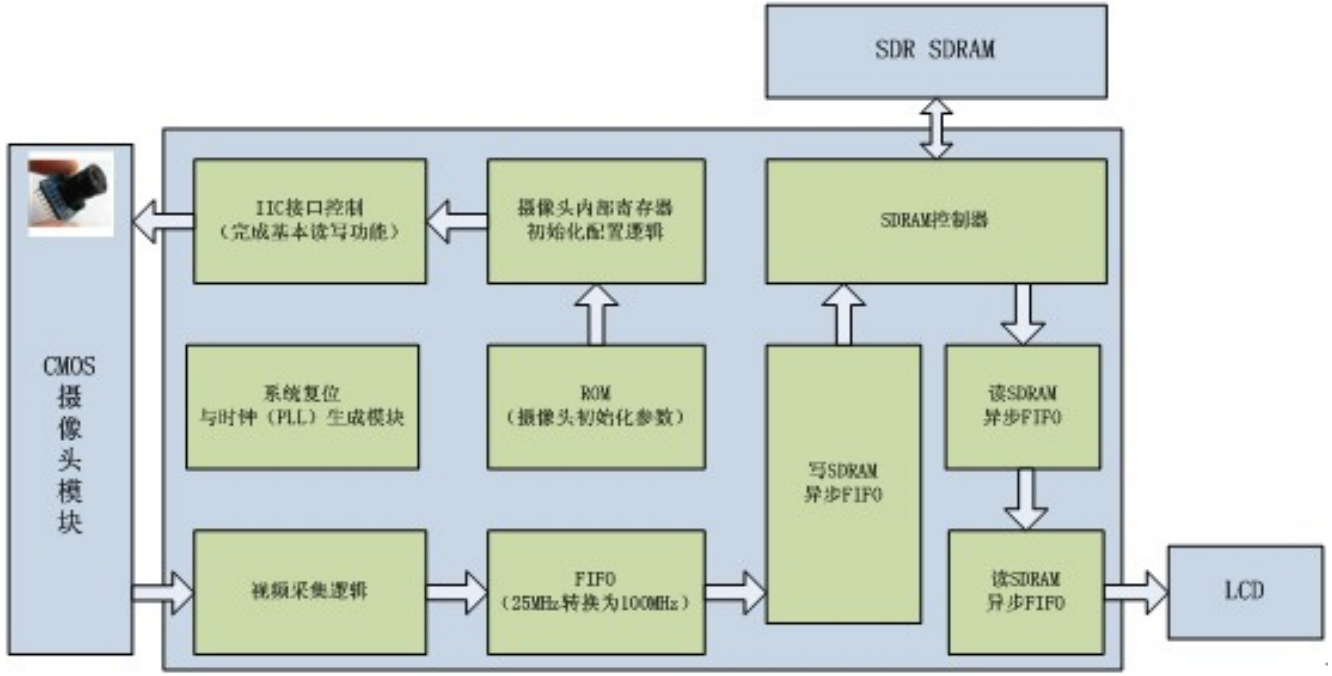
Setup time slack = Data Required Time -Data Arrival Time
Data Arrival Time = Launch Edge + input max delay + Tp2r
Data Required Time = Latch Edge + uTc2r - uTsu

Hold time slack = Data Arrival Time - Data Required Time
Data Arrival Time = Launch Edge + input min delay + Tp2r
Data Required Time = Latch Edge + uTc2r + uTh

时序分析基础

源同步接口输入路径分析实例

—— 系统框图



时序分析基础

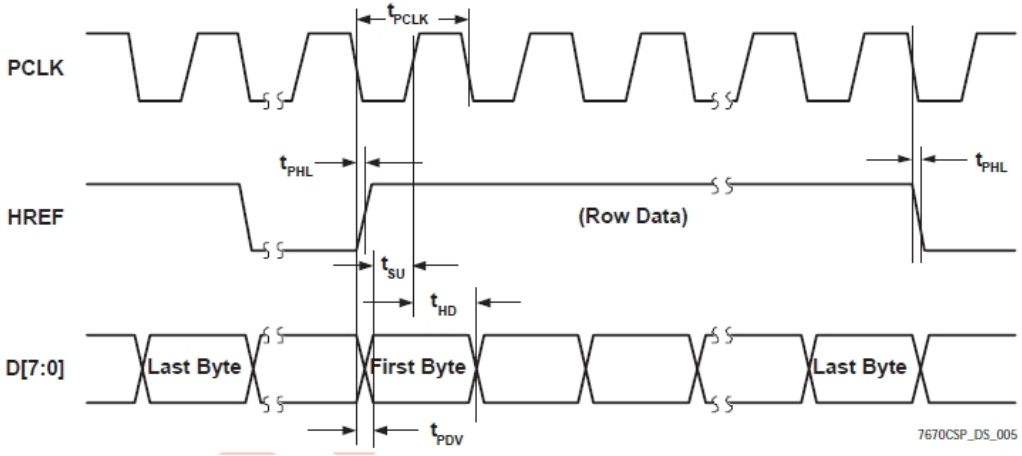
源同步接口输入路径分析实例

—— 实物照片

时序分析基础

源同步接口输入路径分析实例

—— 时钟和数据总线的时序关系

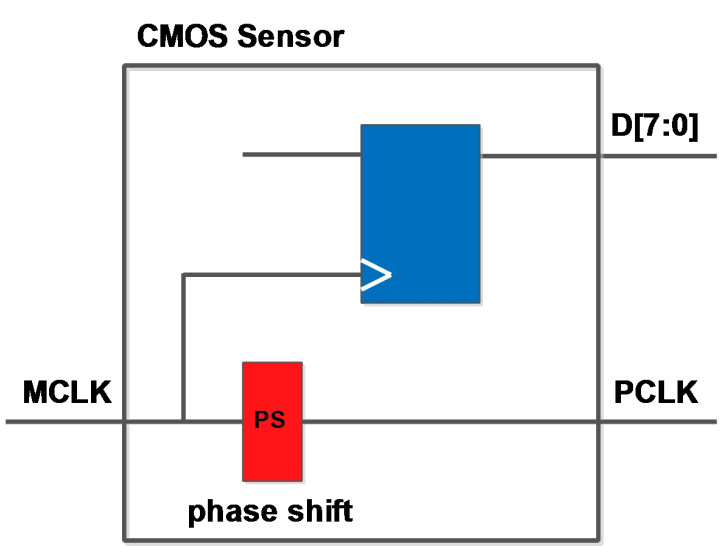


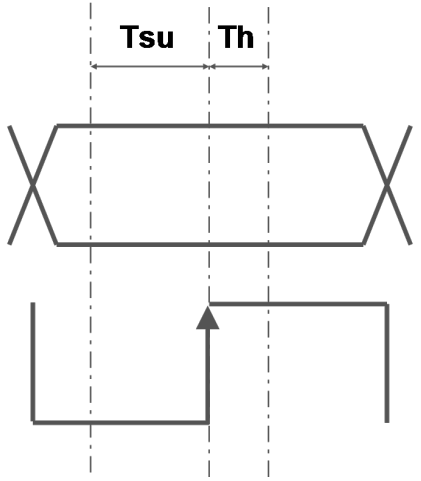
Symbol	Parameter	Min	Typ	Max	Unit
Outputs (VSYNC, HREF, PCLK, and D[7:0] (see Figure 5, Figure 6, Figure 7, Figure 9, and Figure 10)					
t_{PDV}	PCLK[↓] to Data-out Valid			5	ns
t_{SU}	D[7:0] Setup time	15			ns
t_{HD}	D[7:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns

时序分析基础

源同步接口输入路径分析实例

—— 最佳时序采样模型





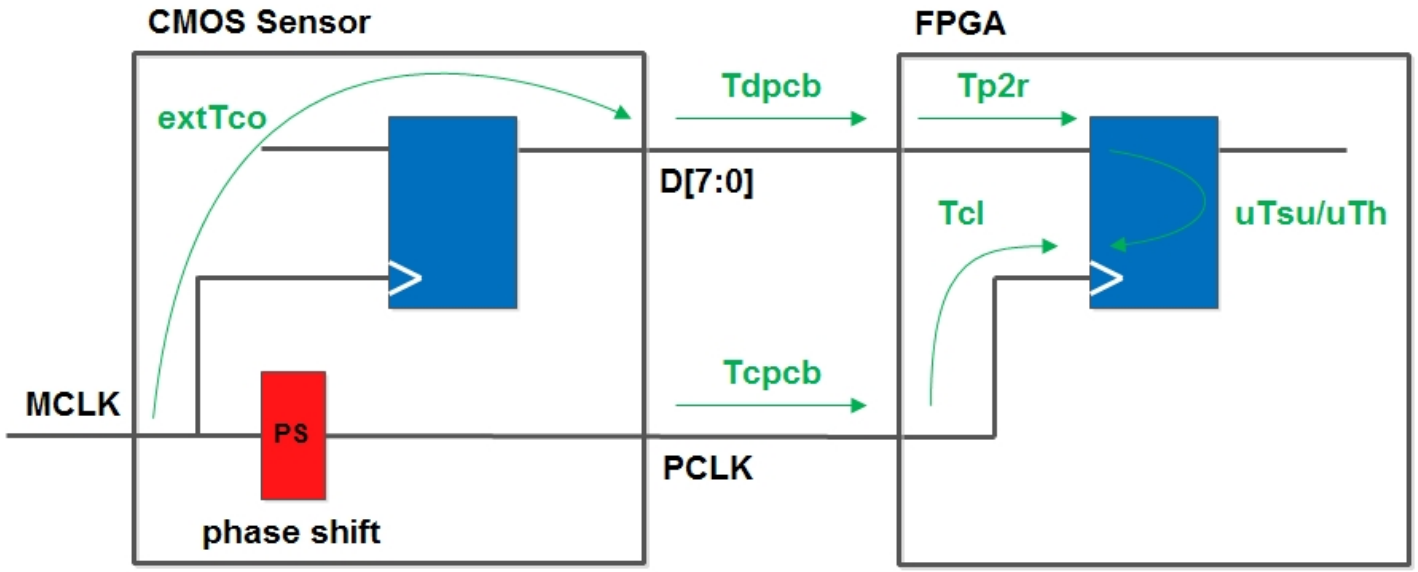
时序分析基础

源同步接口输入路径分析实例

—— 建立时间要求

Launch edge + extTco + Tdpcb + Tp2r

< latch edge + Tcpcb + Tcl - Tsu



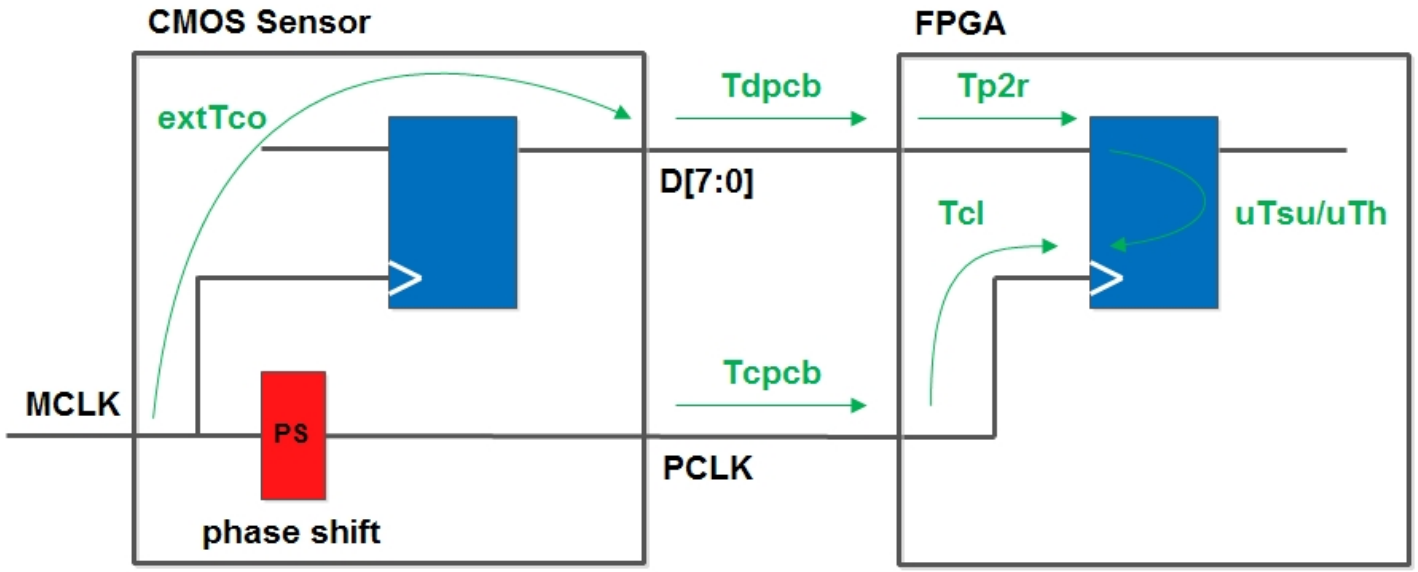
时序分析基础

源同步接口输入路径分析实例

—— 建立时间要求

(Tdpcb – Tcpcb) + extTco

< (latch edge - Launch edge) + Tcl – Tsu -Tp2r



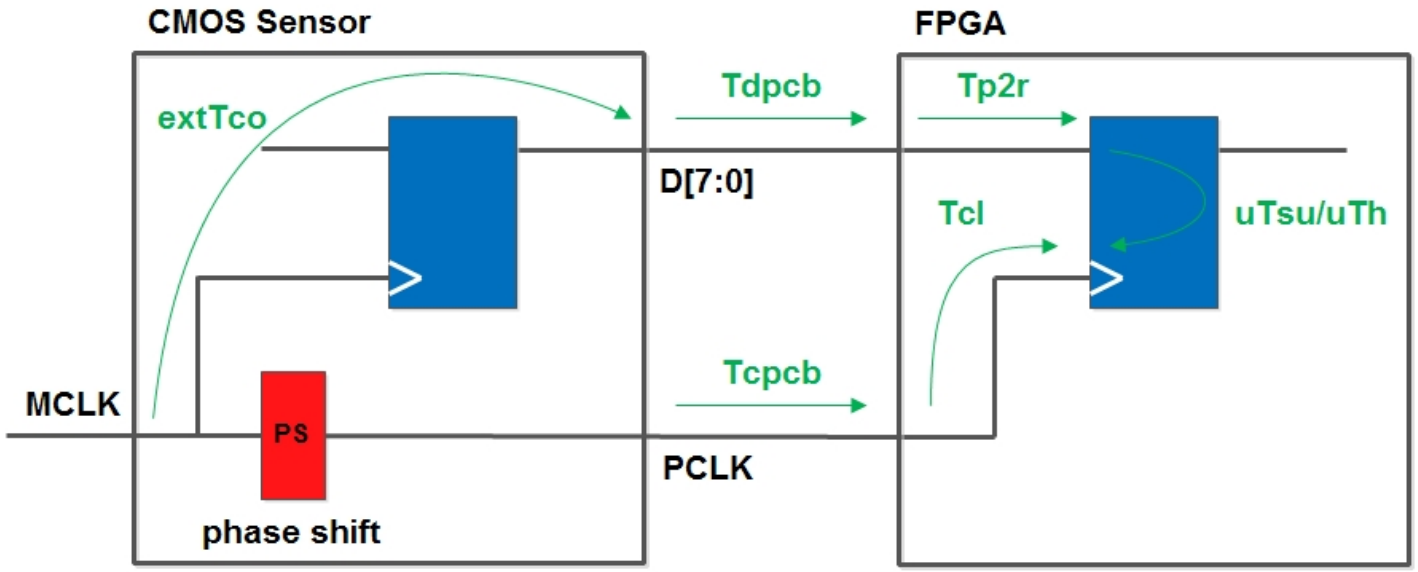
时序分析基础

源同步接口输入路径分析实例

—— 保持时间要求

Launch edge + extTco + Tdpcb + Tp2r

> latch edge + Tcpcb + Tcl - Th



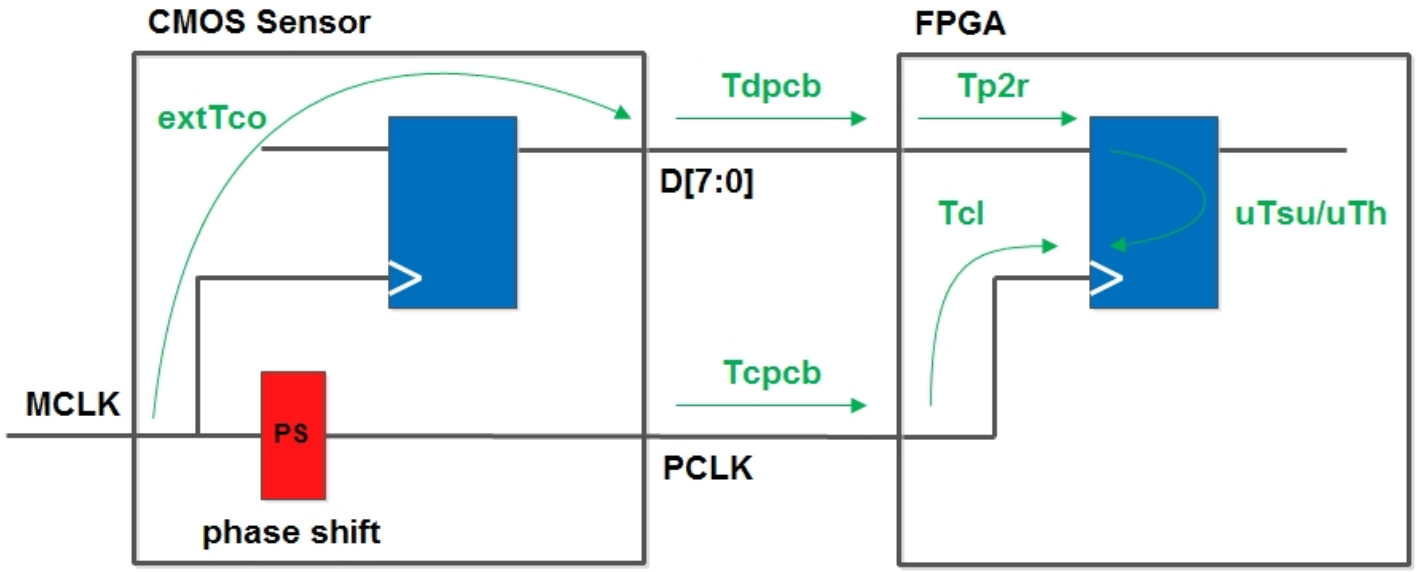
时序分析基础

源同步接口输入路径分析实例

—— 保持时间要求

(Tdpcb – Tcpcb) + extTco

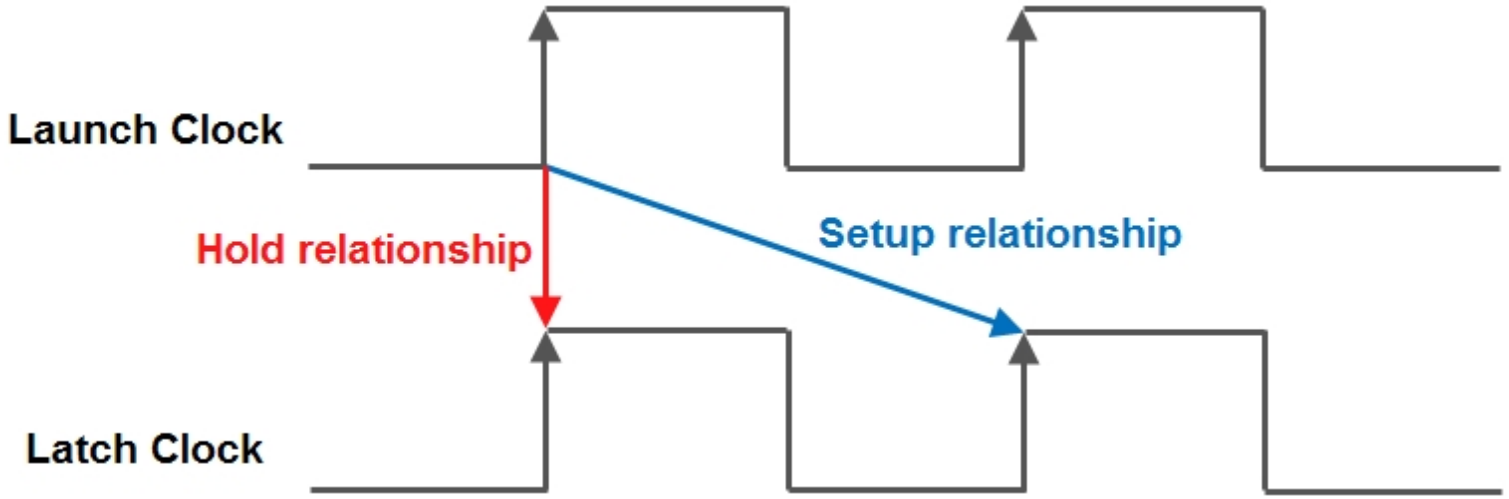
> (latch edge - Launch edge) + Tcl – Th – Tr2p



时序分析基础

源同步接口输入路径分析实例

—— launch edge和latch edge



时序分析基础

源同步接口输入路径分析实例

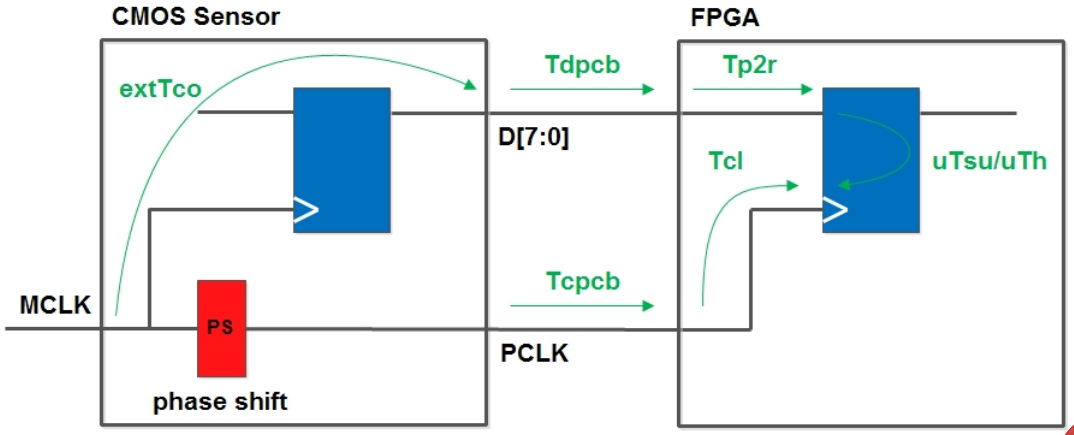
—— set input delay约束参数计算

Input max delay

= (Tdpcb_max – Tcpcb_min) + extTco_max

Input min delay

= (Tdpcb_min – Tcpcb_max) + extTco_min



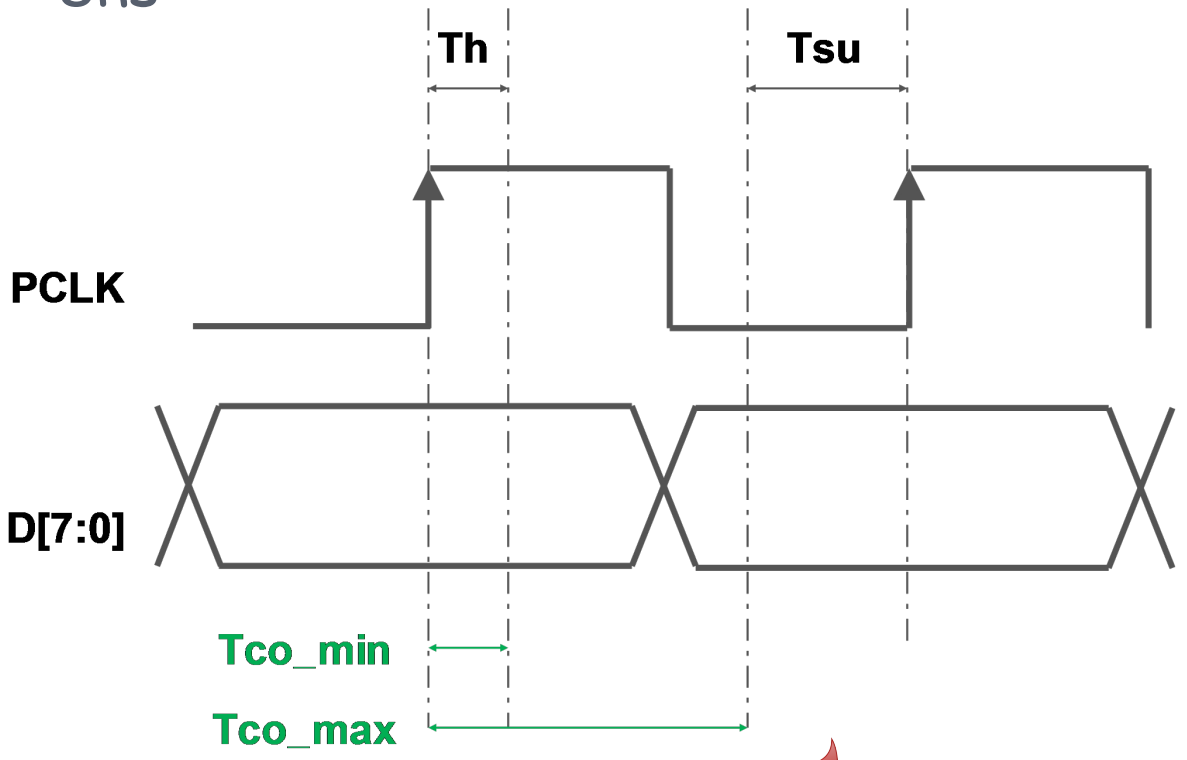
时序分析基础

源同步接口输入路径分析实例

—— Tco的计算

Tco_max = Tpclk - Tsu = 80 - 15 = 65ns

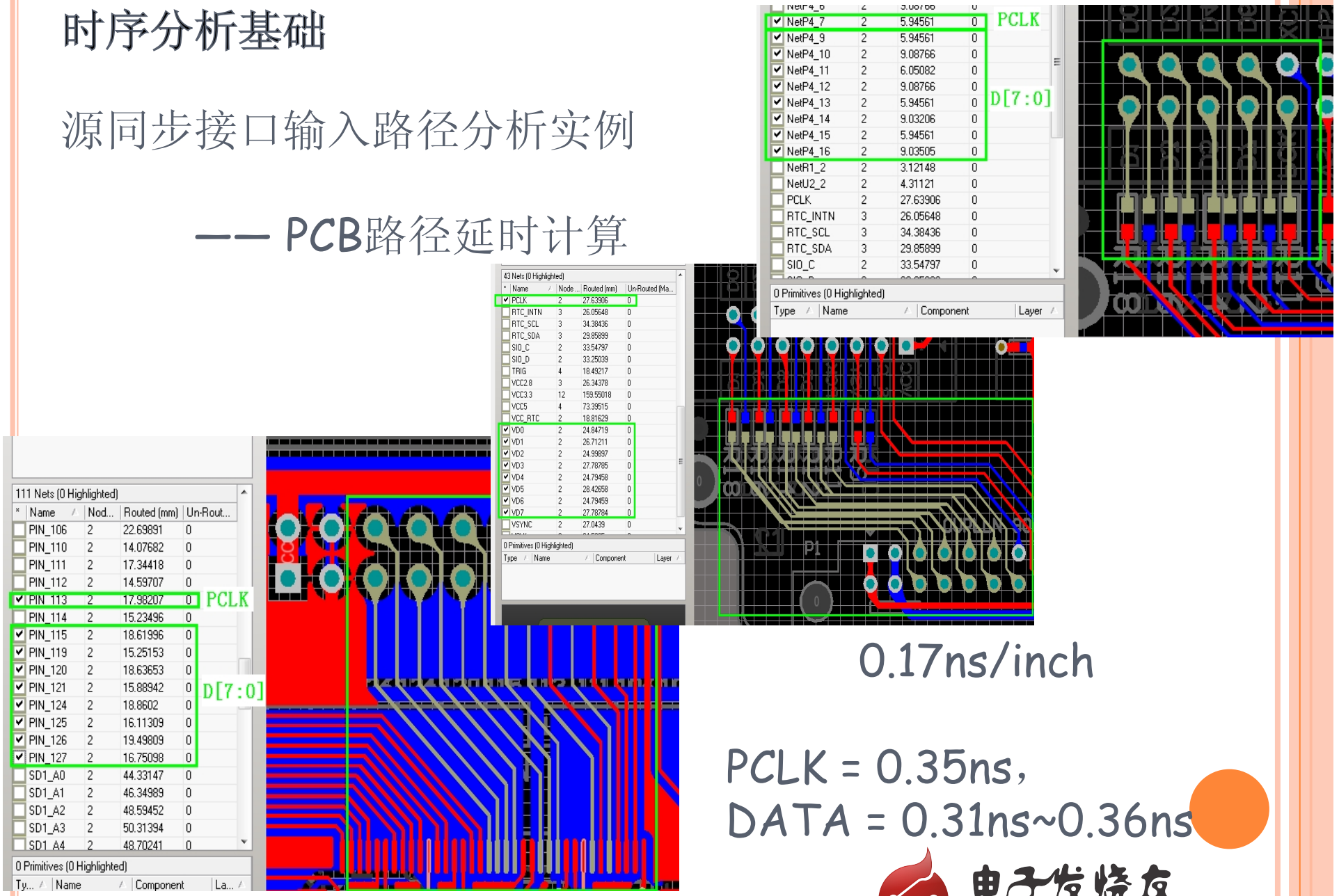
Tco_min = Th = 8ns



时序分析基础

源同步接口输入路径分析实例

—— PCB路径延时计算



时序分析基础

源同步接口输入路径分析实例

—— PCB路径延时计算

Tdpcb_min = 0.31ns
Tdpcb_max = 0.36ns

Tcpcb_min = 0.35ns
Tcpcb_max = 0.35ns

时序分析基础

源同步接口输入路径分析实例

——实际计算

Input max delay
= (0.36ns – 0.35ns) + 65ns = 65.01ns

Input min delay
= (0.31ns – 0.35ns) + 8ns = 7.96ns

取input max delay = 66ns，input min delay = 7ns

时序分析基础

源同步接口输入路径分析实例

——添加约束

VCLK = 12.5MHz

input max delay = 66ns，input min delay = 7ns

时序分析基础

源同步接口输入路径分析实例
——setup路径分析

Setup time slack
= Data Required Time –Data Arrival Time
Data Arrival Time
= Launch Edge + input max delay + Tp2r
Data Required Time
= Latch Edge + uTc2r - uTsu

Path #1: Setup slack is 12.012

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	0.000	0.000					clock path
1	0.000	0.000	R				clock network delay
3	66.000	66.000	F	iExt	1	PIN_127	vdb[0]
4	71.283	5.283					data path
1	66.000	0.000	FF	IC	1	IOIBUF_X16_Y24_N8	vdb[0]~input|i
2	66.927	0.927	FF	CELL	1	IOIBUF_X16_Y24_N8	vdb[0]~input|o
3	71.196	4.269	FF	IC	1	M9K_X27_Y20_N0	uut_videoinput|uut_videoctrl|uut_videofifo|d
4	71.283	0.087	FF	CELL	0	M9K_X27_Y20_N0	video_input:uut_videoinput|video_ctrl:uut_vi

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	80.000	80.000					latch edge time
2	83.227	3.227					clock path
1	83.227	3.227	R				clock network delay
3	83.295	0.068		uTsu	0	M9K_X27_Y20_N0	video_input:uut_videoinput|video_ctrl:uut_vi

时序分析基础

源同步接口输入路径分析实例
——hold路径分析

Hold time slack
= Data Arrival Time – Data Required Time
Data Arrival Time
= Launch Edge + input min delay + Tp2r
Data Required Time
= Latch Edge + uTc2r + uTh

Path #1: Hold slack is 8.259

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	0.000	0.000					clock path
1	0.000	0.000	R				clock network delay
3	7.000	7.000	R	iExt	1	PIN_127	vdb[0]
4	11.850	4.850					data path
1	7.000	0.000	RR	IC	1	IOIBUF_X16_Y24_N8	vdb[0]~input|i
2	7.877	0.877	RR	CELL	1	IOIBUF_X16_Y24_N8	vdb[0]~input|o
3	11.772	3.895	RR	IC	1	M9K_X27_Y20_N0	uut_videoinput|uut_videoctrl|uut_videofifo|d
4	11.850	0.078	RR	CELL	0	M9K_X27_Y20_N0	video_input:uut_videoinput|video_ctrl:uut_vi

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					latch edge time
2	3.337	3.337					clock path
1	3.337	3.337	R				clock network delay
3	3.591	0.254		uTh	0	M9K_X27_Y20_N0	video_input:uut_videoinput|video_ctrl:uut_vi

Thank you